NOIDA INSTITUTE OF ENGINEERING AND TECHNOLOGY, GREATER NOIDA, G.B. NAGAR (AN AUTONOMOUS INSTITUTE)



Affiliated to

DR. A.P.J. ABDUL KALAM TECHNICAL UNIVERSITY, UTTAR PRADESH, LUCKNOW



Evaluation Scheme & Syllabus

For

Bachelor of Technology

Electronics & Communication Engineering (ECE)

Second Year

(Effective from the Session: 2025-26)

NOIDA INSTITUTE OF ENGINEERING & TECHNOLOGY, GREATER NOIDA (AN AUTONOMOUS INSTITUTE)

Bachelor of Technology

Electronics & Communication Engineering

EVALUATION SCHEME

SEMESTER-III

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S. No.	Subject Codes	Subject Name	Type of	1	CITO	122	E	aiuai	ion sene	ines	Semo	ester	Total	Credit
NO.	Codes		Subject	L	T	P	CT	TA	TOTAL	PS	TE	PE		
1	BCSCC0301	Employability Skill Development – I	Mandatory	2	0	0	60	40	100				100	2
2	BASL0301N	Technical Communication	Mandatory	2	0	0	30	20	50		50		100	2
3	BEC0301Z	Digital System Design	Mandatory	2	0	0	30	20	50		50		100	2
4	BEC0302Z	Analog Circuits	Mandatory	3	0	0	30	20	50		100		150	3
5	BEC0306	Data Structures	Mandatory	2	0	0	30	20	50		50		100	2
6	BEC0304	Computational Intelligence	Mandatory	3	0	0	30	20	50		100		150	3
7	BEC0351	Digital System Design Lab	Mandatory	0	0	4				50		50	100	2
8	BEC0352	Analog Circuits Lab	Mandatory	0	0	4				50		50	100	2
9	BEC0356	Data Structures Lab	Mandatory	0	0	2				25		25	50	1
10	BEC0355	IoT Workshop	Mandatory	0	0	6				50		100	150	3
11	BEC0359X	Social Internship	Mandatory	0	0	2				50			50	1
12	BNC0301Y/ BNC0302Y	Artificial Intelligence and Cyber Ethics / Environmental Science	Compulsory Audit	2	0	0	30	20	50				50	NA
		*Massive Open Online Courses (For B.Tech. Hons. Degree)	*MOOCs											
		TOTAL		14	1	18			350	225	350	225	1150	23

* List of MOOCs Based Recommended Courses for Second year (Semester-III) B. Tech Students

Sr. No.	Subject Code	Course Name	University / Industry Partner Name	No of Hours	Credits
1	BMC0012	Data Structures and Algorithms using Python - Part 1	Infosys Wingspan (Infosys Springboard)	29h 27m	2
2	BMC0020	Express PCB Training	Infosys Wingspan (Infosys Springboard)	15h 6m	1

PLEASE NOTE: -

- A 3-4-week Internship shall be conducted during summer break after semester-II and will be assessed during semester-III
- Compulsory Audit (CA) Courses (BNC0301Y/BNC0302Y)
 - ➤ All Compulsory Audit Courses (a qualifying exam) do not require any credit.
 - > The total and obtained marks are not added in the grand total.

Abbreviation Used:

L: Lecture, T: Tutorial, P: Practical, CT: Class Test, TA: Teacher Assessment, PS: Practical Sessional, TE: Theory End Semester Exam., CE: Core Elective, OE: Open Elective, DE: Departmental Elective, PE: Practical End Semester Exam, CA: Compulsory Audit, MOOCs: Massive Open Online Courses.

NOIDA INSTITUTE OF ENGINEERING & TECHNOLOGY, GREATER NOIDA (AN AUTONOMOUS INSTITUTE)

Bachelor of Technology Electronics & Communication Engineering EVALUATION SCHEME

SEMESTER-IV

S.	Subject	Subject Name	Type of Subject	F	Perio	ds	Ev	valuat	ion Schei	mes		nd ester	Total	Credit
No.	Codes	Susgest 1 value	Type of Susjeet	L	T	P	CT	TA	TOTAL	PS	TE	PE		
1	BASCC0401	Employability Skill Development – II	Mandatory	2	0	0	60	40	100				100	2
2	BEC0401	Analog and Digital Communication	Mandatory	3	0	0	30	20	50		100		150	3
3	BEC0403	CMOS Digital Integrated Circuit	Mandatory	3	0	0	30	20	50		100		150	3
4	BEC0402N	Microprocessor & Microcontroller	Mandatory	3	0	0	30	20	50		100		150	3
5		Department Elective 1	Elective	3	0	0	30	20	50		100		150	3
6	BAS0403	Advance Engineering Mathematics	Mandatory	3	1	0	30	20	50		100		150	4
7	BEC0452	Microprocessor & Microcontroller Lab	Mandatory	0	0	4				50		50	100	2
8	BEC0451N	Analog and Digital Communication Lab	Mandatory	0	0	2				25		25	50	1
9	BEC0455	Verilog-HDL	Mandatory	0	0	6				50		100	150	3
10	BCSCC0452	Problèm Solving Approches	Mandatory	0	0	2				50			50	1
11	BEC0459	Mini Project	Mandatory	0	0	2				50			50	1
12	BNC0402Y/ BNC0401Y	Environmental Science / Artificial Intelligence and Cyber Ethics	Compulsory Audit	2	0	0	30	20	50				50	NA
		*Massive Open Online Courses (For B.Tech. Hons. Degree)	*MOOCs											
		TOTAL		18	1	16			350	225	500	175	1250	26

* List of MOOCs Based Recommended Courses for Second year (Semester-IV) B. Tech Students

Sr. No.	Subject Code	Course Name	University / Industry Partner Name	No of Hours	Credits
1	BMC0023	Internet of Things 201	Infosys Wingspan (Infosys Springboard)	15h 59m	1
2	BMC0021	IoT Raspberry Pi with Projects	Infosys Wingspan (Infosys Springboard)	12h 25m	0.5
3	BMC0022	Mobile Apps Development - Advanced Applications	Infosys Wingspan (Infosys Springboard)	14h 23m	1

PLEASE NOTE: -

- A 3-4-week Internship shall be conducted during summer break after semester-IV and will be assessed during Semester-V
- Compulsory Audit (CA) Courses (BNC0401Y/BNC0402Y)
 - ➤ All Compulsory Audit Courses (a qualifying exam) do not require any credit.
 - The Total and obtained marks are not added in the Grand Total.

Abbreviation Used:

L: Lecture, T: Tutorial, P: Practical, CT: Class Test, TA: Teacher Assessment, PS: Practical Sessional, TE: Theory End Semester Exam., CE: Core Elective, OE: Open Elective, DE: Departmental Elective, PE: Practical End Semester Exam, CA: Compulsory Audit, MOOCs: Massive Open Online Courses

List of Departmental Electives

Sr. No.	Departmental Electives	Subject Codes	Subject Name	Bucket Name
1	Elective-I	BEC0412	Introduction to Robotics and it's Applications	Embedded & Robotics
2	Elective-I	BEC0411	Artificial Intelligence	Artificial Intelligence
3	Elective-I	BEC0413	VLSI Technology	Embedded & VLSI

NOIDA INSTITUTE OF ENGINEERING & TECHNOLOGY, GREATER NOIDA (AN AUTONOMOUS INSTITUTE)

Bachelor of Technology Electronics & Communication and Engineering

AICTE Guidelines in Model Curriculum:

A student will be eligible to get Under Graduate degree with Honours only, if he/she completes the additional MOOCs courses such as Coursera certifications, or any other online courses recommended by the Institute (Equivalent to 20 credits). During Complete B.Tech. Program Guidelines for credit calculations are as follows.

1.	For 6 to 12 Hours	=0.5 Credit
2.	For 13 to 18	=1 Credit
3.	For 19 to 24	=1.5 Credit
4.	For 25 to 30	=2 Credit
5.	For 31 to 35	=2.5 Credit
6.	For 36 to 41	=3 Credit
7.	For 42 to 47	=3.5 Credit
8.	For 48 and above	=4 Credit

For registration to MOOCs Courses, the students shall follow Coursera registration details as per the assigned login and password by the Institute these courses may be cleared during the B. Tech degree program (as per the list provided). After successful completion of these MOOCs courses, the students shall provide their successful completion status/certificates to the Controller of Examination (COE) of the Institute through their coordinators/Mentors only.

The students shall be awarded Honours Degree as per following criterion.

- i. If he / she secures 7.50 as above CGPA.
- ii. Passed each subject of that degree program in the single attempt without any grace.
- iii. Successful completion of MOOCs based 20 credits.

~	Code	e: BCSC	CC0301			Course 1	Name: I	<mark>Employa</mark>	bility Sk	ill Deve	<mark>lopment</mark>	– I		L	T	P	C
Course	Offe	red in: l	B.Tech											2	0	0	2
Pre-req	uisite	e: Progra	amming	Languag	ge C												
Course	Obj	jectives:	This c	ourse in	troduces	compu	ter syste	m fund	amentals	, basic	mathema	atics for	com	putin	g, and	softv	vare
develop	nent	principl	es. It en	nphasize	s algoritl	hm desig	n and C	++ progr	ramming	skills. T	Through 1	hands-on	prac	tice a	nd pro	ject-ba	asec
learning	, stu	idents d	evelop	problem	-solving	abilities	and te	amwork	while	creating	real-wo	rld appl	icatio	ns, r	nini-ga	ames,	and
simulation	ons, e	enhancir	ng both t	echnical	and coll	aborative	e compet	encies		_							
Course	Outo	come: A	fter com	pletion o	of the cou	urse, the	student	will be al	ble to					Bloc	om's K	nowle	dge
				-										Leve	el (KL)	
CO1	Ap	ply sets,	relation	s, function	ons to co	mputatio	onal prob	lem-solv	ving						K	3	
CO2		derstand								cycle us	ing logic	al reason	ning				
CO2	and	d flowch	arts.	-	•					•			Ū		K	3	
CO3		sign and		-	scale so	ftware p	projects	or game	s using	structure	ed progra	amming	and		K	6	
	•	oject-bas													17	.0	
CO4		llaborate					present	a comp	plete sof	tware pr	oject, de	emonstra	ting		K	6	
		oblem-so					`										
		pping (S	cale 1: I	Low, 2: I	Vledium	, 3: High	1)		1	1	1						
CO-PC		PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO	1 1	PSO2	PSC)3
Mappi	ng																
CO1		3	3	2	2	-	-	-	2	-	-	-	-		-	-	
CO2		3	3	3	2	-	-	-	2	-	-	-	-		-	-	
CO3		3	3	3	2	_	_	_	2	_	_	_	_		_	1 _	
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CO4		3	3	3	3	-	-	-	2	-	-	-	-		-	-	
		tents / S	yllabus														
Module											al Conce					hour	
	-	ystem F						-	-					-	_		
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Mathen Inductio	n and		in proof														5
_	n and		in proof		ware Do	evelopm	ent Fun	damenta	ıls						6	hour	
Mathen Inductio Module Introduc	n and 2 tion	d its use	are Dev	Soft elopmen	t Life Cy	cle, Step	-by-step	solution	to simp	le proble	ms, Dev	eloping l	ogic/f	lowc			ode
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Course Offe	e: BASL03				Course I		Technic	al Com	municat	tion			LT	P C
						BS)							2 0	0 2
Pre-requisite		diate le	vel (CE	FR) and	d above									
Course Obje														
	nonstrate (on skill	s in dive	erse profe	ssional s	ettings, i	ncluding	5
	tings, pres			-				•44			1	.,	1	
	elop and a						_	te writt	en comi	nunicatio	on, sucn	as emaii	s, letters	,
	ipt commu							nal. and	l situati	onal con	texts to f	oster inc	lusive	
	respectful		•			, -		,						
	ploy digita							ideo cor	nferenci	ng, busine	ess messa	aging ap	ps) respo	nsibly
and	effectively	in remo	ote or hy	brid wo	rk envir	onment	s.							
Course Outo	ome: Afte	r comple	etion of	the cou	rse, the s	student v	vill be a	ble to						
	nend the pr							on.						
	r specific a													
	ze and prod fective spe							nirses						
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CO-PO Map	ping (Sca	le 1: Lo	w, 2: M	edium,	3: High)								
СО-РО	DO1	DO2	DO2	DO4	DO5	DO.	DO7	DOG	DOG	DO10	DO11	DCO1	DCO1	PGG
Mapping	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	1	1	1	1	1	2	1	1	2	3	1	2	_	_
CO2	1	1	1	1	1	1	1	1	2	3	1	2	_	_
CO3	1	1	1	1	1	1	1	1	2	3	1	2	_	_
CO4	1	1	1	1	1	1	1	1	2	3	1	2		
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Course Cont	tents / Syll	abus	T4	J4	4- T1	!1.0	1	4					4 TT	
Module 1			intro	auction	to Tech	ınıcaı C	ommur	ucation					4 Hours	
Technical Co	ommunica	tion: De	efinition	, Proces	ss, Type	s, Level	s, and F	low; Ba	rriers t	o Techni	cal Com	municat	ion: em	phasis on
gender neutra														•
Module 2			Tech	nical W	riting 1								5 Hours	
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Technical with Minutes of Module 3 Job applicate Plagiarism Module 4	Meetings	me'; Rep	port, pr	oposal; c Speak	Technic	cal pape						ing, Refe	erencing 6 Hours	and
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- 1. Technical Communication, 15th Edition by John M. Lannon & Laura J. Gurak, Pearson, 2021.
- 2. Spoken English- A Manual of Speech and Phonetics (5th Edition) by R K Bansal & J B Harrison, Orient Blackswan, 2024, New Delhi.
- 2024, New Delhi.
 Business Correspondence and Report Writing by Prof. R C Sharma, Krishna Mohan, and Virendra Singh Nirban (6 Edition), Tata McGraw Hill & Co. Ltd., 2020, New Delhi.

Intercultural Communication in Virtual Exchange by Francesca Helm, Cambridge Univ. Press, 2024.

inter-cartarar c	Sommanication in Virtual Exchange of Transcoscationin, Cambridge Cinv. 11655, 2021.
NPTEL/ You	tube/ Faculty Video Link:
Module 1	https://onlinecourses.nptel.ac.in/noc24_ge37/preview
Module 2	https://archive.nptel.ac.in/courses/109/106/109106094/
Module 3	https://www.youtube.com/watch?v=kOJlwMJxEG0&t=8s
Module 4	https://www.youtube.com/watch?v=Sg7Q_dC_fWU&list=PLPuC5CMHiqmuzq_KQ4aw0V9Q7xJY6aezb
Module 5	https://www.youtube.com/watch?v=ymLFJDpjgCk&list=PLPuC5CMHiqmuzq_KQ4aw0V9Q7xJY6aezb&index=6

		e: BEC03				Course	Name:	Digital	System	Design				L	T	P	C
Course	Offer	red in: B	.Tech. E	CE/VL	SI									2	0	0	2
Pre-requ	uisite	: Basic c	oncept of	f numbe	r systei	ms, Boo	olean Al	gebra, D	igital lo	gic fami	lies.						
	_	ctives: T					_					-	_	-		_	_
and anal	ysis o	of combin	national a	ınd sequ	ential c	ircuits,	Synchr	onous &	Asynch	ronous S	Sequentia	al Circuit	s, Semic	onduc	ctor m	emori	es
and prog	gramn	nable log	ic device	es.													
Course	Outco	ome: Aft	er compl	letion of	the cou	urse, the	e studen	t will be	able to					Bloo	m's K	nowl	edg
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CO5	PLI		concept	or seini	Conduc	tor Me	mories	and mip	nement t	ne digit	ai logic	runctions	using		K	4	
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CO-P						, ,	1										
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CO	3	3	3	2	-	-	-	-	-	-	-	-	1		2	2	2
CO ₄	4	3	3	2	-	_	-	-	-	-	-	-	1		2	2	2
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Module Number Forms, F Module Code Co	Syste <u>Karna</u> 2 onversor, Se	ems, Con lugh Map	nplement s upto 5 mparator	s of Nur Variable Com s, Adde Adders,	mbers, es, Mul bination ers: Ha	Boolean tilevel 1 onal Log If Adde Adder, 1	n Algeb NAND/I gic Circ er, Full Multiple	ra, De M NOR rea cuits Adder, exers, De	Morgan's alizations Carry L emultiple	s, Binary ook Ah	Codes.	ler, Subt	ractors:		orms, 8 Subtra	Canor hour ctor,	rs nica rs Fu
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Module Number Forms, F Module Code Co Subtracto Module Sequenti and T Ty	Syste Carna 2 conversion, Se 3 (al Cinype F)	ems, Con augh Map resion, Cor erial And recuits Fur lip Flops,	mplements upto 5 mparator Parallel ndamenta , Excitati	Variable Com rs, Adders, Sequents: Basion and o	mbers, es, Multiples, Multiples, Multiples, Harbert BCD Activation and the characters where the control of the	Boolean tilevel Nonal Log If Adder, Nonal Logic a	n Algeb NAND/I gic Circ er, Full Multiple nd Its A	ra, De M NOR reacuits Adder, exers, De Applicat	Morgan's alizations Carry Lemultiple ions al circuit	ook Ah exers, En	ead Add coders, a	ler, Subtand Deco	ractors: ders.	Half K, JK	Subtra	Canon hour hour hour hour Shour	rs Fu
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2	"Digital Electronics- An introduction to theory and practice", PHI, 2nd edition ,2006.	W.H. Gothmann
3	Theory and Logic Design", PHI, 2013.	A. Anand Kumar
NPTEL/Y	Youtube/ Faculty Video Link:	
Module 1	https://www.youtube.com/watch?v=juJR_JDJRa0	
Module 2	https://www.youtube.com/watch?v=sUutDs7FFeA	
Module 3	https://www.youtube.com/watch?v=ibQBb5yEDlQ	
Module 4	https://www.youtube.com/watch?v=ntiv1g7G_C4	
Module 5	https://www.youtube.com/watch?v=4GpWA_hmRhw	

Course Co	ode: BEC)302Z			Course	e Name	e: Analo	og Circu	uits				L	T	P	\mathbf{C}
Course Of	ffered in:	B.Tech	ECE/VL	SI									3	0	0	3
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CO1	Design and	l analyz	e the diffe	erent tra	nsistor a	amplifi	er circui	its.						•	<u>-/</u> {4	
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CO2	3	3	3	1	-	-	-	-	-	-	-	2	2		1	
CO3	3	3	3	-	-	-	-	-	-	-	-	2	2		2	
CO4	3	3	2	2	-	-	-	-	-	-	-	3	3		2	
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Course Co	ontents / S	yllabus														
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3	Analysis and Design of Analog Integrated Circuits, John Wiley, 3rd Edition	Paul R.Gray & Robert G.Meyer									
NPTEL/Y	NPTEL/ Youtube/ Faculty Video Link:										
Module 1	https://www.youtube.com/watch?v=2bprLH4cUSo										
Module 2	https://www.youtube.com/watch?v=XDy-rD5AJI0										
Module 3	https://www.youtube.com/watch?v=dHSaPhQIQqE										
Module 4	https://nptel.ac.in/courses/117101106										
Module 5	https://www.youtube.com/watch?v=2bprLH4cUSo										

Course Code: BEC0306	Course Name: Data Structure	L	T	P	C
Course Offered in: ECE		2	0	0	2

Pr-requisite: Knowledge of C, data types and their organization.

Course Objectives: This course focuses on the basic concepts of algorithm analysis, along with implementation of linear and non-linear data structures and file structures.

Course	Outcome: After completion of the course, the student will be able to	Bloom's Knowledge				
		Level (KL)				
CO1	Understand the concept of time and space complexity along with the linear data structure array	K2				
CO1	and linked lists.	KZ				
CO2	Understand the concept of stack and queue with their memory representations.	K2				
CO3	Apply the knowledge of the nonlinear data structure- tree and their operation.	K3				
CO4	Analyze the basics of graph with their different traversal ways.	K4				
CO5	Apply the concepts of searching, sorting and file structure.	K3				

CO-PO Mapping (Scale 1: Low, 2: Medium, 3: High)

CO-PO Mapping	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	3	2	2	2	-	-	-	-	2	-	3	2	1
CO2	3	3	3	1	2	-	-	-	-	1	-	3	2	1
CO3	3	3	3	2	2	-	-	-	-	1	-	3	3	1
CO4	3	3	2	2	2	-	-	-	-	1	1	3	3	2
CO5	3	3	3	3	2	-	-	-	-	2	1	3	3	2

Course Contents / Syllabus

UNIT 1 Introduction to data structures, Arrays and Linked lists 8 hours

Introduction: Basic Terminology, Elementary Data Organization, Built in Data Types in C/python. Algorithm, Efficiency of an Algorithm, Time and Space Complexity, Asymptotic notations: Big Oh, Big Theta and Big Omega, Abstract Data Types (ADT) Arrays: Single and Multidimensional Arrays, Representation of Arrays: Row Major Order, and Column Major Order, Index Formulae for 1-D,2-D,3-D and n-D Array Application of arrays, Sparse Matrices and their representations.

Linked lists: Array Implementation of Singly Linked Lists, Doubly Linked List, Circularly Linked List, Operations on a Linked List. Insertion, Deletion, Traversal. Polynomial Representation and Addition Subtraction & Multiplications of Single variable.

UNIT 2 Stack and Queues 8 hours

Stacks: Abstract Data Type, Primitive Stack operations: Push & Pop, Array and Linked Implementation of Stack, Application of stack: Prefix and Postfix Expressions, Evaluation of postfix expression, Iteration and Recursion- Principles of recursion, Tail recursion, Removal of recursion Problem solving using iteration and recursion with examples of binary search, Fibonacci numbers, and Hanoi towers. Tradeoffs between iteration and recursion.

Queues: Operations on Queue: Create, Add, Delete, Full and Empty, Circular queues, Dequeue and Priority Queue.

UNIT 3 Trees 8 hours

Basic terminology used with Tree, Binary Trees, Binary Tree Representation: Array Representation and Pointer (Linked List) Representation, Binary Search Tree, Strictly Binary Tree, Complete Binary Tree, An Extended Binary Trees. Tree Traversal algorithms: In-order, Pre-order and Post-order. Constructing Binary Tree from given Tree Traversal, Operation of Insertion, Deletion, Searching & Modification of data in Binary Search tree, Introduction of Binary Heaps, Threaded Binary trees, Traversing Threaded Binary trees, AVL Tree, B-Tree.

UNIT 4 Graphs 8 hours

Graphs: Terminology used with Graph, Data Structure for Graph Representations, Adjacency matrices, Adjacency List. Graph Traversal: Depth First Search and Breadth First Search. Connected Component, Spanning Trees, Minimum Cost Spanning Trees: Prim's and Kruskal's algorithm. Shortest Path algorithms: Dijkstra Algorithm.

UNIT 5 Searching and Sorting 8 hours

Searching: Concept of Searching, Sequential search, Index Sequential Search, Binary Search, Concept of Hashing.

Sorting: Insertion Sort, Selection, Bubble Sort, Quick Sort, Merge Sort, Heap Sort and Radix Sort.

File Structure: Concepts of files, records and files, Sequential, Indexed and Random File.

	To	otal Lecture Hours 40 hours				
Textbook	:	<u> </u>				
S.No	Book Title with publication agency & year	Author				
1	"Data Structures and Algorithms in Python: An Indian Adaptation", 1st Edition, 2021.	Michael T. Goodrich, Roberto Tamassia				
2	"Fundamentals of Data Structures", Computer Science Press, 1st Edition, 1993.	Horowitz and Sahani				
3	"Data Structures" Schaum's Outline Series, Tata McGraw-hill Education (India) Pvt. Ltd, 2nd Edition, 2017.	Lipschutz				
Reference	Books:					
S.No	Book Title with publication agency & year	Author				
1	"Data Structure Using C", Oxford University Press, 2nd Edition, 2014.	Reema Thareja				
2	"Data Structure Using C", Pearson Education India, 2nd Edition,2011.	AK Sharma				
3	"C and Data structure", Wiley Dreamtech Publication, 1st Edition, 2004.	P. S. Deshpandey				
NPTEL/	Youtube/ Faculty Video Link:					
Module 1	https://www.youtube.com/watch?v=zWg7U0OEAoE&list=PLBF3763AF2E1C572F https://www.youtube.com/watch?v=LQx9E2p5c&pp=ygUMYXJyYXlzIG5wdGV: https://www.youtube.com/watch?v=K7VIK1Udo20&pp=ygUPbGluayBsaXN0IG5w	s				
Module 2	https://www.youtube.com/watch?v=g1USSZVWDsY&list=PLBF3763AF2E1C572Fhttps://www.youtube.com/watch?v=g1USSZVWDsY&list=PLB3CD0BBB95C1BF0	2F&index=2				
Module 3	https://www.youtube.com/watch?v=tORLeHHtazM&list=PLBF3763AF2E1C572F&https://youtu.be/tORLeHHtazM?si=rPsohifPQuFaJXg4	zindex=6				
Module 4	https://www.youtube.com/watch?v=9zpSs845wf8&list=PLBF3763AF2E1C572F&ir	ndex=24				
Module 5	https://www.youtube.com/watch?v=4OxBvBXon5w&list=PLBF3763AF2E1C572F&					
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	https://www.youtube.com/watch?v=KW0UvOW0XIo&list=PLBF3763AF2E1C572I	F&index=5				

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Discuss the concept of genetic algorithm and its various applications. K2												
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COS 3 2 Course Contents / Syllabus

Mapping CO1

CO₂

CO3

CO4

Module 1 Introduction to Computational Intelligence

8 hours

Introduction to Computational Intelligence, Various types of Computational Intelligence Techniques, Characteristics of Computational Intelligence, Major Areas of Computational Intelligence, Applications of Computational Intelligence. Introduction to MATLAB / Python Environment for Computational Intelligence Techniques.

Module 2 Neural Networks

8hours

Neuron, Biological neurons and its working, Model of Artificial Neuron, Architectures, Taxonomy of ANN Systems, Various Activation Functions, Single Layer ANN System, Multi-Layer ANN System, Recurrent networks. Supervised Learning, Unsupervised Learning, Reinforcement Learning, Perceptron, Adaline, Madaline, and Applications of ANN in research. MATLAB Neural Network Toolbox / Python.

Module 3 Fuzzy Logic-I

8 hours

Fuzzy Set theory, Operations on sets, Properties, Fuzzy versus Crisp set, Fuzzy Relation, Operations on Fuzzy Relation, Properties, Fuzzy versus Crisp Relations, Introduction & features of membership functions, Max-Min Composition.

Module 4 Fuzzy Logic-II

8 hours

Introduction to Fuzzy logic, Propositions, If-Then Rules, implications and inferences. Rule based systems, Predicate logic, Fuzzy Inference Systems, Fuzzification, Defuzzification Method, logic controller design, Some applications of Fuzzy logic. Fuzzy Logic MATLAB Toolbox/Python

Module 5 Genetic Algorithm (GA)

8 hours

Fundamentals of Genetic Algorithms, Basic concepts, Working Principle, Various Encoding methods, Fitness function, GA Operators-Reproduction, Crossover, Mutation, Convergence of GA, Bit wise operation in GA, Optimization of traveling salesman problem using Genetic Algorithm, Genetic Algorithm MATLAB Toolbox/Python, Hybrid Computational Intelligence

Total Lecture Hours	40 hours

Textbook		
S.No	Book Title with publication agency & year	Author
1	"Computational Intelligence: An Introduction", Wiley Publication.Data	
	Structures and Algorithms in Python (An Indian Adaptation), Wiley	Andries P. Engelbrecht
	Publication (15 July 2014)	

2	"Neural Networks, Fuzzy Logic and Genetic Algorithm: Synthesis and Applications", Prentice Hall of India.	S. Rajsekaran & GA Vijayalakshmi Pai									
3	"Neural Netowrks", Prentice Hall of India	Siman Haykin									
4	"Fuzzy Logic with Engineering Applications", Wiley India.	Timothy J. Ross									
Refer	ence Books:										
S.No	Book Title with publication agency & year	Author									
1	"Neural Networks", Tata Mc Graw Hill.	Kumar Satish									
2	"Computational Intelligence and Intelligent System Design: Theory Tools and applications", Pearson.	Fakhreddin O. Karray, Clarence W. De Silva									
NPTEL/	NPTEL/ Youtube/ Faculty Video Link:										
Module 1	https://youtu.be/fgtUFzxNztA?si=DiEQ7L2PNrQvgC5y										
Module 2	https://www.youtube.com/watch?v=xbYgKoG4x2g&list=PL53BE265CE	4A6C056									
Module 3	https://www.youtube.com/watch?v=K7S3TgfqnX0&list=PLFW6lRTa1g8	31F7CJ-CdlsyWKKAa43T62j									
Module 4	https://www.youtube.com/watch?v=JrRWdPvG7yk&list=PLFW6lRTa1g8	81F7CJ-CdlsyWKKAa43T62j&index=2									
Module 5	https://www.youtube.com/watch?v=d86McbWXh4E&list=PLwdnzlV3og	oWyi7exLIe26JhueiVQXq_S									

LAB Cour	rse Code:	BEC03	51		LA	B Cou	rse Na	me: Dig	ital Syst	em Desigr	Lab		L	T	P	C
Course Of	fered in: 1	B.Tech	ECE/\	/LSI									0	0	4	2
Pre-requis					c opera	tions,	Basics of	of decim	al numbe	er system						
Course Ol		•			•					-						
The studer																
combination					d verif	ication	of truth	table o	f various	type of fli	p-flops. I	Designing	and im	plem	entati	on of
different ty																
Course O	utcome: A	fter con	pletion	n of the	course	e, the s	tudent v	vill be al	ole to						Knowl	edge
													Leve			
CO1	Verify tru														<u> </u>	
CO2	Design, in														<u> </u>	
CO4													<u> </u>			
	CO4 Design and implement different types of sequential logic circuits. K CO-PO Mapping (Scale 1: Low, 2: Medium, 3: High)												<u>.</u> 4			
			LOW, 2	. Wicus	J.	lingin										
CO-PO Mappin	1 201	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSC	2	PSO	13
									2							
CO1	3	3	3	-	2	-	_	3	2 2	-	2	1	2 2		2	
CO2	3	2	3	_	2	_	_	3	2	_	2	1	2		2	
CO4	3	3	3	_	2	_	_	3	2	_	2	1	2		2	
												1				
List of Pra	actical's (I	ndicati	ve & N	ot Lin	nited T	(o)										
1. Verifica	`						nd Univ	ersal I c	oric Gate	s using TT	I ICs					
	ND (7408)		0105 01	Dusic	Logic (Juics u	na cinv	CISUI DC	gie Guie	s using 11	L ICs.					
	R (7432)	,														
1	OT (7404)	1													C)1
	AND (740															
	OR (7402)	· ·														
2. Impleme			en Boo	lean fu	nction	using 7	TTL Los	gic Gate	s (NOT.	AND and	OR Gates) in SOP fo	or			
following 1		_				0	- (,	,			,				
_	1 = AB' +	-													CO) 1
b) Y	2 = ABC +	A'B'C	' + A'	C												
c) F	(A, B, C, I	$\Sigma(0) = \sum_{i=1}^{n} (0)^{i}$,2,5,7,	8,10,13	,15)											
3. Impleme						using 7	TL Log	gic Gate	s (NOT,	AND and	OR Gates)) in POS fo	orms			
for followi	ng Boolea	n expres	sions:													
a) Y	1 = (A' + B))(A+B'))												CO) 1
b) Y	2 = (A + B +	+C)(A'+	B'+C')(A'+C	()											
	(A, B, C, E)),2,5,7,	8,10,12	2,15)											
4. Impleme		•													C) 1
4-bit Binar																<i>J</i> 1
5. Impleme AND-7408						Full-ad	der usin	ig two H	lalf – add	ler with TT	L Logic (Gates (EX	OR-74	86,	CO	02
6. Impleme	entation of	Half-su	btracto	r, Full-	-subtra				r using tv	wo Half-su	btractor w	vith TTL L	ogic		CO)2
Gates (EX)	OR-7486, entation of	AND-74 4-bit Pa	408, Ol trallel a	K-7432 adder 11	() and v	erify it	s truth t	able.	utput for	the given	inputs.					
	= 1011, B			u	₆ /=		, (1)	, 0		51,011	P 440.				C) 2
b) A	= 0011, B	= 0010														
8. Implements its truth talk		2:4 Dec	coder, 1	:4 Der	nultiple	exer us	ing Log	ic Gates	(NOT g	ate- 7404,	AND gate	e- 7408) aı	nd veri	fy	C)2

9. Implementation of 4:2 Encoder , 4:1 multiplexer using logic gate (OR gate-7432) and verify its truth table.	CO2
10. Implement and verify $F(A,B,C) = \sum (3, 5, 6, 7)$ using	
a) 8:1 multiplexer.	CO2
b) 4:1 multiplexer.	
11. Implement 2 Bit magnitude comparator using logic gates and verify the truth table.	CO2
12. Verification of truth table of flip-flop using NAND gate (7400) & NOR gates (7402).	
a) RS Flip Flop	
b) JK Flip Flop	CO3
c) D Flip Flop	
d) T Flip Flop	
13. Implement D flip flop using SR flip flop and verify the truth table.	CO3
14. Design and implement 4-bit ring counter using D flip flop and verify the result.	CO3
15. Design MOD 5 asynchronous counter using T flip flop and verify the truth table.	CO3
16. Design MOD 5 synchronous counter using T flip flop and verify the truth table.	CO4
17. Realize	
a) Design Mod – N Synchronous Up Counter & Down Counter using 7476 JK Flip-flop	CO4
b) Mod-N Counter using IC7490 / 7476	CO4
c) Synchronous counter using IC74192	
18. Design Pseudo Random Sequence generator using 7495.	CO4

Lab Course Offered in: B.Tech ECEVISI Course Offered in: B.Tech ECEVISI Pre-requisite: The operation and characteristics of semiconductor devices.																	
Pre-requisite: The operation and characteristics of semiconductor devices. Course Objectives: The course aims to equip students with knowledge and hands-on experience in designing, implementing, and verifying various characteristics of transistor amplifiers. It also focuses on the design and implementation of diverse applications of operational amplificrs. Qn-amplificrs. Qn-amplificrs. Additionally, students will learn to simulate cletronic circuits using simulation software and gain an introduction to circuit design using PCB design software such as PCB Express and KiCad. COID Design and profession of the course, the student will be able to Evel (KL) CO2 Design and verify Op-Amp base circuits K4 CO3 Design and verify Op-Amp base circuits K4 CO3 Design and unplementation of oscillators. K4 CO3 Design and unplementation of oscillators. K4 CO4 Simulate the Electronic circuits on simulation software. K3 CO5 Design and implement electronics circuits by PCB design software (PCB Express. Ki cad). K4 CO6 Design and implement electronics circuits by PCB design software (PCB Express. Ki cad). K4 CO7 OMapping PO1 PO2 PO3 PO4 PO5 PO6 PO7 PO8 PO9 PO1 PO1 PS01 PS02 PS03 CO1 OMapping Scale I: Low. Ver. Medium. 3: High) CO2 Design and implement electronics circuits by PCB design software (PCB Express. Ki cad). K4 CO3 Solidary So	LAB Cou	rse Code:	BEC03	52		LAB Co	ourse Na	me: An	alog Cir	cuit Lal	b			L	T	P	С
Course Objectives: The course aims to equip students with knowledge and hunds-on experience in designing, implementing, and verifying various characteristics of transistor amplifiers. It also focuses on the design and implementation of diverse applications of operational amplifiers (Op-amps) and oscillators. Additionally, students will learn to simulate electronic circuits using simulation software and gain an introduction to circuit design using PCB design software such as PCB Express and KiCad. Course Outcome: After completion of the course, the student will be able to Bloom's Knowledge Level (KL)	Course Of	ffered in:	B.Tech	ECE/VI	SI									0	0	4	2
verifying various characteristics of transistor amplifiers. It also focuses on the design and implementation of diverse applications of operational amplifiers (Op-amps) and oscillators. Additionally, sudents will learn to simulate electronic circuits using simulation software and gain an introduction to circuit design using PCB design software such as PCB Express and KiCad. Course Outcome: After completion of the course, the student will be able to Bloom's Knowledge Level (KL) CO1 Design and plot frequency response of amplifiers K4 CO2 Design and reify Op- Amp base circuits by PCB design software such as PCB Express, Ki and K4 CO3 Design and implementation of oscillators. CO4 Simulate the Electronic circuits on simulation software. CO3 Design and implement electronics circuits by PCB design software (PCB Express, Ki cad). CO4 Simulate the Electronic circuits on simulation software. CO3 Design and implement electronics circuits by PCB design software (PCB Express, Ki cad). CO4 Simulate the Electronics circuits by PCB design software (PCB Express, Ki cad). K4 CO5 Design and implement electronics circuits by PCB design software (PCB Express, Ki cad). K4 CO5 Design and implement electronics circuits by PCB design software (PCB Express, Ki cad). K4 CO6 Design and implement electronics circuits by PCB design software (PCB Express, Ki cad). K4 CO7 Design and implement electronics circuits on simulation software. CO8 Design and implement electronics circuits by PCB design software (PCB Express, Ki cad). K4 CO9 Design and implement electronics circuits on simulation software. CO9 Design and software (PCB Express, Ki cad). K4 CO9 Design and position (PCB Express, Ki cad). K4 CO9 Design and position (PCB Express, Ki cad). K4 CO9 Design and software (PCB Express, Ki cad). K4 CO9 Design and software (PCB Express, Ki cad). CO9 Design and software (P	Pre-requis	site: The o	peration	and cha	racteristi	cs of ser	nicondu	ctor devi	ces.								
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Software and gain an introduction to circuit design using PCB design software such as PCB Express and KiCad. Course Outcome: After completion of the course, the student will be able to Bloom's Knowledge Level (KL) CO1 Design and plot frequency response of amplifiers K4 CO2 Design and plot frequency response of amplifiers K4 CO3 Design and plot frequency response of of scillators. K4 CO4 Simulate the Electronic circuits on simulation of scillators. K3 CO5 Design and implement electronics circuits by PCB design software (PCB Express, Ki cad). K4 CO5 Design and implement electronics circuits by PCB design software (PCB Express, Ki cad). K4 CO-PO Mapping (Scale I: Low, 2: Medium, 3: High) This post of PCB Express, Ki cad). K4 CO-PO Mapping (Scale I: Low, 2: Medium, 3: High) This post of PCB Express, Ki cad). K4 CO1 3 3 1 - 2 2 2 2 2 1 2 2 CO1 3 3 1 - 2 2 2 2 2 1 2 2 <td< td=""><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></td<>																	
Colimage														uits u	ısing	simul	ation
CO1										ich as Po	CB Expre	ess and k	KiCad.				
CO2	Course O	utcome: A	After com	ipletion o	of the co	urse, the	student	will be a	ble to								edge
CO2	CO1	Design a	nd plot f	requency	respons	se of amı	plifiers								K	4	
CO5 Design and implement electronic circuits by PCB design software (PCB Express, Ki cad). K4																	
CO-PO Design and implement electronics circuits by PCB design software (PCB Express, Ki cad). K4	CO3	Design a	nd imple	ementatio	on of osc	illators.									K	4	
CO-PO Mapping (Scale 1: Low, 2: Medium, 3: High)	CO4														K	3	
PO1 PO2 PO3 PO4 PO5 PO6 PO7 PO8 PO9 PO10 PO11 PSO1 PSO2 PSO3															K	4	
Mapping PO1 PO2 PO3 PO3 PO5 PO6 PO7 PO8 PO7 PO7 PO8 PO7 PO7 PO8 PO7	CO-PO M	lapping (S	cale 1:	Low, 2:	Medium	, 3: Hig	<u>h)</u>		_	_	_						
CO1 3 3 3 1 - 2 2 2 - 2 2 2 2 1 2 2 2 2 2 2 2 2 2		PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO0	PO10	PO11	PSO	1 D	SO2	DC	03
CO2	Mapping	101	102	103	104	103	100	107	100	10)	1010	1011	150	1 1	302	10	03
CO3 3 3 2 - 2 2 - 2 2 2 2 1 2 2 CO4 3 3 2 - 3 2 - 2 2 2 2 2 2 1 2 2 List of Practical's (Indicative & Not Limited To) List of Practical's (Indicative & Not Limited To) 1. Design and implement a CE (BC-107) amplifier with potential divider biasing (for Vi = 20 mV, R1=100KΩ R2=10KΩ, RC= 4.7 KΩ, RE=1KΩ). Verify the following parameters with the theoretical values: a) Voltage gain Av b) Current gain Ai c) Input Resistance (Ri) d) Output Resistance (Ri) d) Output Resistance (Ri) d) Output Resistance (Ri) CO1 a) Bandwidth b) Input impedance c) Maximum signal handling capacity (MSHC). c) Maximum signal handling capacity (MSHC). c) Maximum signal handling capacity (MSHC). 3. Design a single-stage CE and a multistage (CE-CE) amplifiers with Voltage Divider Bias for 10 mV input ac signal and plot the Frequency Response curves using BC 547, VCC = 12V, Stability factor (S) =10 and RL= 10 KΩ. Observe the effect on gain and bandwidth input and output impedance. CO1 5. Design voltage series Feedback amplifier with basic voltage gain 100 and feedback factor 0.1-0.2 a	CO1	3	3	1	-	2	2	-	2	2	2	2	1		2		2
CO4	l 			1	-	+	-	-		-	-	1	1				2
List of Practical's (Indicative & Not Limited To)			+		-	1	+	-		-							
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b) Current gain Ai c) Input Resistance (Ri) d) Output Resistance (Ro) 2. Design and analysis of Single stage common source MOSFET amplifier with potential divider biasing (for Vi = 20 mV, Rl=1MΩ R2=1 KΩ, RD= 4.7 KΩ, Rs=1 KΩ) and Plot Gain (dB) Vs frequency curve, also measure following parameters a) Bandwidth b) Input impedance c) Maximum signal handling capacity (MSHC). 3. Design a single-stage CE and a multistage (CE-CE) amplifiers with Voltage Divider Bias for 10 mV input ac signal and plot the Frequency Response curves using BC 547, VCC = 12V, Stability factor (S) =10 and RL=10 KΩ. Observe the effect on gain and bandwidth. 4. Design current series/Voltage shunt Feedback amplifier with basic voltage gain 100 and feedback factor 0.1-0.2 also analyze the effect of feedback on gain, bandwidth input and output impedance. 5. Design Voltage series Feedback amplifier with basic voltage gain 100 and feedback factor 0.1-0.2 also analyze the effect of feedback on gain, bandwidth, input and output impedance. 6. Design and analyze the output voltage V0 for OP-AMP (IC 741) as: a) Inverting and Non-inverting amplifier for input voltage 0.5V with input Resistance (Ri) of 10 KΩ and feedback Resistance (Rf) of 100 KΩ. b) Voltage follower circuits for input voltage 1V. 7. Design a differential amplifier with ±12V DC power supply and calculate Common mode gain, differential mode gain, CMRR and slew-rate. 8. Design and analyze OP-AMP applications as a difference amplifier, integrator and differentiator Circuits for 1 KHz input signal.	· ·			,	J		<i>J</i> 1										
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	8. Design	and analyz		MP appl	ications	as a diff	ference a	mplifier	, integrat	or and o	lifferenti	ator Circ	uits fo	r 1 K	Hz	C)2
			d output	wavefor	ms of a g	given ful	l wave p	recision	rectifier.							C	<u></u>

10. Design and implement of 2nd order Active Low pass filter for cut-off frequency 1KHz and pass band gain of 1.586, also draw the frequency response curve and verify cutoff frequency.	CO2					
11. Design and implement of 2nd order Active High pass filter for cut-off frequency 1KHz and pass band gain of 1.586, also draw the frequency response curve and verify the cutoff frequency.	CO2					
12. Design the following RC sinusoidal oscillators; Also verify the theoretical and practical Oscillating frequency.						
a) RC phase shift oscillator, if its frequency of oscillation is 955 Hz and R1=R2=R3 =680K Ω .	CO3					
b) Wien bridge oscillator uses $R=4.7K\Omega$, $C=0.01\mu F$, and $RF=2R1$	CO3					
13. Design the following LC oscillators; Also verify the theoretical and practical Oscillating frequency.						
a) For a Hartley oscillator, self-inductance of the two coils are L1=100mH, L2=1mH and mutual inductance						
between the two coils is 20µH. its output for a capacitor of value 20pF.	CO3					
b) For a Colpitts oscillator in which feedback network consists of two capacitors of 100 pF and 20 pF with 100 mH coil across these capacitors.						
14. Design and implement square wave generator (Astable Multivibrator) for 1 MHz using,						
a) Op-amp	CO3					
b) IC 555.						
15. Design and implement a triangular wave generator using dual op-amp, for oscillation frequency $f_0 = 1.5$ KHz and Vout (P-P) =6V, use Vsat = 13.5 V.	CO3					
16. Design and simulate single-stage CE amplifiers with Voltage Divider Bias for 10mV input ac signal and plot the						
Frequency Response curves using BC 547, VCC= 12V, Stability factor (S)=10 and RL= 10 KΩ. (TARGET, PSPICE-	CO4					
letc.)						
17. Simulation of Multistage stage (CE-CE) amplifier (designed in experiment1) using any available simulation software and also find the Voltage gain, Input impedance, Output impedance, and bandwidth. (TARGET, PSPICE-1etc.)	CO4					
18. Design and simulate current series/Voltage shunt Feedback amplifier with basic voltage gain 100 and feedback factor 0.1-0.2 also analyze the effect of feedback on gain and bandwidth.	CO4					
19. Design and simulate Voltage series Feedback amplifier with basic voltage gain 100 and feedback factor 0.1-0.2 also analyze the effect of feedback on gain and bandwidth.	CO4					
20. Design and simulate of 2nd order Active Low pass filter for cut-off frequency 1KHz and pass band gain of 1.586, also draw the frequency response curve and verify the cutoff frequency.	CO4					
21. Design and simulate of 2nd order Active High pass filter for cut-off frequency 1KHz and pass band gain of 1.586, also draw the frequency response curve and verify the cutoff frequency.	CO4					
22. Identification of various types of Printed Circuit Boards (PCB) and soldering Techniques.	CO5					
23. PCB Lab: Artwork & printing of a simple PCB.	CO5					
24. Etching & drilling of PCB.	CO5					
25. Wiring & fitting shop: Fitting of power supply along with a meter in cabinet.	CO5					
26. Mini Project: Design a mini project using the applications of this Lab.	CO5					
27. Identification of various types of Printed Circuit Boards (PCB) and soldering Techniques.						
Total Hou	ırs: 40 hrs.					

LAB C	ourse	Code: B	EC0356	6		LAB C	ourse I	Name: 1	Data St	ructure	Lab			L	T	P	C		
Course	Offer	ed in: B.	Tech. F	ECE/VI	.SI									0	0	2	1		
						ing con	cepts us	sing C/C	C++ and	underst	tanding o	f fundan	nental algo	·					
													ays, linked			s, que	ues,		
trees, ar	ıd grap	hs. It ain	ns to en	hance p	roblem-	solving	abilitie	s throug	h effici	ent algo			code opti						
Course	Outco	ome: Afte	er comp	oletion o	etion of the course, the student will be able to Bloom'											Know	ledge		
														Leve	el (KI	ر)			
CO1	_	lementin niques.	g Single	e and M	ulti-dim	ensiona	l array	with the	ir appli	cations	like searc	ching and	d Sorting		k	<u> </u>			
CO2													K 3						
CO3	Implementation of tree data structures for basic operations like insertion, deletion, searching and												7.1						
COS	traversal.												. 4						
CO4	Implementation and analysis of various operation like searching, sorting, hashing in data structures K4											74							
	for solving real world problems. PO Mapping (Scale 1: Low, 2: Medium, 3: High)												• •						
		ping (Sca	de 1: L	ow, 2: N	<u> ledium</u>	1, 3: Hig	gh)	1	1	1	1	1							
CO-Po		PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PS	O2	PS	03		
CO1		3	2	3	2	3	-	-	-	-	2	-	3	3	3	1			
CO2		3	3	3	2	3	-	-	-	-	1	-	3	3	3	1			
CO3		3	3	3	2	3	-	-	-	-	1	-	3	3	3	1			
CO4		3	3	3	3	3	-	-	-	-	2	1	3	3	3	2			
List Of	Pract	ical's (In	dicativ	e & Not	t Limite	ed To)													
S.No							Progr	am Des	criptio	n							CO		
1	Cons	truct a co	de to fi	nd the n	naximur	n eleme										_	CO1		
2		truct a co							rray.								CO1		
3	Cons	truct a co	de to re	verse th	e eleme	nts of a	n array.		-							(CO1		
4	Cons	truct a co	de to co	ount the	occurre	nce of a	specifi	c eleme	nt in an	array.						(CO1		
5		truct a co									lumn ma	jor order	•				CO1		
6		am to fin								atrix.							CO1		
7		truct a co															CO1		
8		truct a Py						s using 1	ecursio	n.							CO2		
9		truct a co		_												_	CO2		
10 11		truct a pr truct a pr						,									CO2		
12		truct a pr						<u>′·</u>									CO2		
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Write a program to implement an in-order traversal of a binary tree and print the nodes.

Write a program to implement a pre-order traversal of a binary tree and print the nodes.

Write a program to implement a post-order traversal of a binary tree and print the nodes.

Write a program to count number of nodes in a binary tree.

Write a Program to search a number in Binary Search Tree (BST).

Write a program to delete a node from a Binary Search Tree (BST).

Write a program to perform Depth-First Search (DFS) on a graph.

Write a program to perform Breadth-First Search (BFS) on a graph.

Construct a program to implement merge sort with recursion and iteration.

Write a program to insert a node in a Binary Search Tree (BST).

Write a program to find the height of the tree.

Write a program to implement Prims Algorithm.

Write a program to implement Kruskal Algorithm.

Write a program to implement Dijkstra Algorithm.

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	Total Hour	s: 48 hrs.
35	Write a program to implement a max-heap and perform heap sort on an array of integers.	CO4
34	Construct a program to implement bubble sort.	CO4
33	Construct a code to implement binary search.	CO4
32	Construct a code to implement linear search.	CO4
31	Construct a program to implement quick sort with recursion and iteration.	CO4

	: BEC0	355			Cour	se Nam	e: IoT V	V <mark>orkshop</mark>	I	, <u> </u>	Т			P
					(Woı	rkshop N	Mode)							
Course Offer									()	0		(6
Pre-requisite														
Course Obje	ectives:	To prov	ide stud	lents wit	th a goo	d depth	of know	wledge o	f Desig	ning Indi	ustrial Io	T System	ms for v	arious
applications.														
Course Outc	ome: A	ter comp	oletion of	f the cou	rse, the s	tudent w	ill be ab	le to			Bloon (KL)	n's Know	ledge Le	vel
CO1					•		pportMo	duleies	and be	nefits in	_ ` ′	K	 [1	
CO2				Appl		network	to demo	nstrate th	e use of	Cloud in		K		
CO3				To ar		DC/DAC				mponents			[4	
CO4				Expla	ain the co		nd use of	em design various I		ocols and		K		
CO5				Anal	yze chall		nd issues		IoT Sec	curity and		K	[4	
CO-PO Map	ping (So	cale 1: L	ow, 2: N				cicty pro	oiciis.						
СО-РО			<u> </u>				DO#	DOG	DOG	DO10	DO11	DGO1	DG O A	DG 0.2
Mapping	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
BEC0355.1	3	2	2	-	-	-	-	-	-	-	-	3	2	2
BEC0355.2	3	3	3	_	_	_	_	_	_	_	_	3	2	-
BEC0355.3	3	2	3	_	_	_	_	_	_	_	_	3	2	-
BEC0355.4	3	2	1	-	-	-	-	-	_	-	-	3	2	_
BEC0355.5	3	2	1	-	-	-	-	-	_	-	-	3	2	-
Course Cont	ents / Sy	llabus					I.	<u> </u>		I I		I.	I.	l
Module 1					Introd	uction to	o IoT an	d IIoT ar	nd its ba	asic funda	amental	s: 8 ho	ours	
Introduction t														
and Benefits				Workfor	ce – Lo	gistics ar	nd the In	dustrial I	nternet-	IoT Inno	vations i	n Retail.	Introduct	tion to
Integrated De Module 2	veloped	Environ	ments.		Common	Networ	1					8ho		
	or Notu	orka, Ui	stom: on	d Contav				odas Na	tuvorlein	a Modos	WCN on			iool
Wireless Sens Systems (CPS														
bystems (Cr	,	-				BDIT (E	onware	Defined i	10000011	us) The C	oroug une	.105 1	tole of Bi	5
•						o and R	aspberr	y pi Prog	grammi	ng		8 hc	ours	
Data in HoT -		T.							•	*			dvanced	data
Data in HoT - Module 3 ADC and DA Viewpoints			pology:											
Data in IIoT - Module 3 ADC and DA Viewpoints - analytics.			pology:		IoT Se	curity a	nd Proto	ocols				8 ha	ours	
Data in HoT - Module 3 ADC and DA Viewpoints - analytics. Module 4	Archite	ctural To				curity a			RT NF	C Z-Way	ve. Bacne	8 ho		
Data in HoT - Module 3 ADC and DA Viewpoints - analytics. Module 4 Wireless Tecl	Archite	ctural To	: WPAN	I Techno	logies fo	r IoT: IE	EEE 802.	15.4, HA				et, Modbu	ıs.	curity,
Data in HoT - Module 3 ADC and DA Viewpoints - analytics. Module 4 Wireless Tecl IP Based Pro Threat Model	Archite	ctural To	: WPAN	I Techno	logies fo RPL, RE	or IoT: IE ST, AM	EEE 802. PQ, CoA	15.4, HA				et, Modbu	ıs.	curity,
Data in HoT - Module 3 ADC and DA Viewpoints - analytics. Module 4 Wireless Tecl IP Based Pro Threat Model	Archite	ctural To	: WPAN	I Techno	logies fo RPL, RE	r IoT: IE	EEE 802. PQ, CoA	15.4, HA				et, Modbu	is. s, IoT Sec	curity,
Data in HoT - Module 3 ADC and DA Viewpoints - analytics. Module 4 Wireless Tecl IP Based Pro Threat Model Module 5 Smart Cities,	Archite hnologie tocols fo	s for IoT IP	T: WPAN Pv6, 6Lov Managen	I Techno wPAN, I	logies for RPL, RE Applice gistics, A	or IoT: IE ST, AM ations of Agricultu	EEE 802. PQ, CoA	15.4, HA	Γ. Edge	connecti	vity and	et, Modbu protocols	is. s, IoT Secours	
Data in HoT - Module 3 ADC and DA Viewpoints - analytics. Module 4 Wireless Tecl IP Based Pro Threat Model Module 5 Smart Cities,	Archite hnologie tocols fo	s for IoT IP	T: WPAN Pv6, 6Lov Managen	I Techno wPAN, I	logies for RPL, RE Applice gistics, A	or IoT: IE ST, AM ations of Agricultu	EEE 802. PQ, CoA	15.4, HA	Γ. Edge	Robot su	vity and	et, Modbu protocols 8 ho ee, Indust	os, IoT Secondrial IoT,	
Data in IIoT - Module 3 ADC and DA Viewpoints - analytics. Module 4	Archite hnologie tocols fo	s for IoT IP	T: WPAN Pv6, 6Lov Managen	I Techno wPAN, I	logies for RPL, RE Applice gistics, A	or IoT: IE ST, AM ations of Agricultu	EEE 802. PQ, CoA	15.4, HA	Γ. Edge	connecti	vity and	et, Modbu protocols 8 ho ee, Indust	is. s, IoT Secours	
Data in HoT - Module 3 ADC and DA Viewpoints - analytics. Module 4 Wireless Tecl IP Based Pro Threat Model Module 5 Smart Cities, challenges, Ice	Archite hnologie tocols fo	s for IoT IP	T: WPAN Pv6, 6Lov Managen	Techno wPAN, I ment, Lo chvironm	Applic gistics, Aental Produino Cargolis,	ations of Agricultustection.	EEE 802. PQ, CoA f IoT re, Heal k, 3rd ed Ap	15.4, HA AP, MQT th and Li Edition	Γ. Edge festyle, T by M 0.Publis	Robot su Cotal Lect Sichael Cotal Lect Cotal Lect Cotal Lect Cotal Lect Cotal Lect Cotal Lect	vity and	et, Modbu protocols 8 ho ee, Indust	ours trial IoT,	Legal

	Communications", Cambridge University Press,						
	2005.						
2	Raspberry Pi Cookbook, 4th Edition Released	Simon Monk					
	December 2022.Publisher(s): O'Reilly Media, Inc.	Simon Work					
Reference Books:							
1	Internet of Things: Principles and	Rajkumar Buyya, Amir Vahid					
	Paradigms, Morgan Kaufmann, 2016.	Dastjerdi					
NPTEL/ Youtube/ Faculty Video Li	nk:						
Module 1	https://www.youtube.com/watch?v=om-5QTbl	LCCs					
Module 2	https://www.youtube.com/watch?v=BBvG7uzr	mOV0&t=51s					
Module 3	https://www.youtube.com/watch?v=HicZcgdG	xZY&t=39s					
Module 4	https://www.youtube.com/watch?v=-7dAFWRjCoA						
Module 5	https://www.youtube.com/watch?v=SW3Ia5xI	<u>LmuU</u>					

List of Practical's	(Indicative & Not Limited To)	
S.NO	Name of Experiment	Cos
1	Study of IDE and practice of its installation.	CO1
2	Create a traffic light signal with three coloured lights (Red, Orange and Green) with a duty cycle of 5-2-10 seconds.	CO 2
3	Simulation of 4-Way Traffic Light with Arduino	CO 2
4	Working with Adafruit Libraries in Arduino.	CO 2
5	Connect an LED to GPIO pin 25 and control it through the command line.	CO 2
6	The state of LED should toggle with every press of the switch Use DHT11 temperature sensor and print the temperature and humidity of the room with an interval of 15 seconds.	CO 2
7	To study Libraries and their installation.	CO 3
8	To interface a servo motor with an Arduino board and control its position using PWM signals.	CO 3
9	To learn how to interface a DC motor with an Arduino board and control its speed and direction.	CO 3
10	To understand how to interface a relay with an Arduino board and control external devices.	CO 3
11	To understand how to interface a stepper motor with an Arduino board and control its rotation.	CO 3
12	To detect the presence of LPG or propane gas using the MQ-6 gas sensor and Arduino.	CO 3
13	Study and Installation of Raspberry Pi.	CO 3
14	Displaying different LED Patterns with Raspberry Pi.	CO 3
15	Programming of available GPIO Pins of the corresponding device using native programming language. Interfacing LED and testing the functionality.	CO 3
16	To explore BLE communication and data exchange.	CO 4
17	Home automation system	CO 5
18	Health care system	CO 5
19	Smart Irrigation System	CO 5

20	Electric Piano	CO 5
21	Design and simulate of 2nd order Active High pass filter for cut-off frequency 1KHz and pass band gain of 1.586, also draw the frequency response curve and verify the cutoff frequency.	CO4
22	Identification of various types of Printed Circuit Boards (PCB) and soldering Techniques.	CO5
23	PCB Lab: Artwork & printing of a simple PCB.	CO5
24	Etching & drilling of PCB.	CO5
25	Wiring & fitting shop: Fitting of power supply along with a meter in cabinet.	CO5
26	Mini Project: Design a mini project using the applications of this Lab.	CO5
27	Identification of various types of Printed Circuit Boards (PCB) and soldering Techniques.	CO5
		Total Hours: 40 hrs.

Course C	ode: BN	C0401	Y		C	Course N	ame: A	rtificia	al Intellg	ence and	Cyber E	thics	L	T	P	C
Course O	ffered in	: B. Te	ch.										2	0	0	2
Pre-requi	isite: Bas	ic unde	erstand	ling of	AI, Cy	bercrim	e, Com	puter S	System a	nd Ethic	S		•	•		
	Course Objectives: The course aims to foster critical thinking about ethical issues, promote responsible use of technology, and ensure students can identify, analyze, and address ethical dilemmas in Artificial Intelligence and cyber domains.														,	
										Artificia	l Intellige	nce and c				
Course O	utcome:	After c	omplet	ion of t	he cour	se, the st	tudent v	will be a	able to					om's I		ledge
	· 1			C A T	.1 .			.1 . 1	• •	.•	1 11 .			el (KL	ر.)	
	Learn ke developn		-		ethics,	summar	ızıng e	thical (considera	ations an	d applicat	ions in A	.1	K	2	
CO2	Apply policies and framework for Fairness in AI and Machine Learning. K3															
	and Cyber Security.															
CO4 Understand the nature of cybercrimes, the principles of intellectual property rights (IPR), and the legal measures necessary to address and prevent these issues.																
CO-PO Mapping (Scale 1: Low, 2: Medium, 3: High)																
CO-PO PO1 PO2 PO3 PO4 PO5 PO6 PO7 PO8 PO9 PO10 PO11 PSO1 PSO2 PSO3																
Mapping CO1	3 101	1	100	101		1	2	100	10)	1010	2	1	1	1		
CO2	2	3	2	_	2	1	2	-	2	1	2	2	1	1		
CO3	2	3	2	1	2	3	3	-	2	2	2	2	2	1		
CO4	2	2	_	_	1	3	3	_	2	2	2	2	1	1		
Course Contents / Syllabus																
Module 1 An Overview to AI Ethics 6 hours													rs			
Definition of AI Ethical principles in AI, Sources of AI data, Legal implications of AI Security Breaches, Privacy and AI Regulations,																
Key Principles of Responsible AI, Transparency and Accountability, Dual-Use Dilemma, Human-Centric Design, Introduction to																
Cyber Lav	ws and Et	hics, H	istorica	l Deve	lopmen	t of Cybe	er laws,	Legal	framewo	rks.						
Module 2	,			Fairne	ess and	Favorit	ism in	Machir	ne Learn	ing				1	3 hou	rs
Introducti																
Fairness a										neworks	for Fairne	ess in AI,	Bias in	Data	Colle	ction,
Fairness in Module 3		ocessin	g, Gen			d Cybers									3 hou	rs
Importance and Privace	ce of Privacy-Preser	ving Da	ata Min	ty in A ing (PF	I, AI sp DM), I	ecific Se Risk Mar	curity ageme	Tools a nt: Risk	nd Softw Assessr	nent and	Incident R	esponse, l	Regulato	rning	(PPM	IL)
GDPR, H		ise Stuc	iies: Im			, IPR an				practices	in engine	ering proj	ects.		3 hou	rs
Types of	Cybercrir	nes and	their	Impact,	Legal	measures	s for C	ybercrii	ne Preve	ention and	l Prosecut	ion, IPR:	Copyrig	hts, T	raden	narks.
Patents, ar				-					•	•	•				_	
and Digita												Compara	tive Ove	rview	: Indi	an vs
Global Cy	ber Laws	s, Case	Study:	The A	M Hei	st – Cosi	nos Ba	nk Cyb	er Attack	(India, 2	-					
Torrth a al-	•]	Total Lect	ure Hou	ırs (30 ho	urs
Textbook S.No	.:	Boo	ok Title	e with j	publica	tion age	ncy &	year				Autho	r			
1.			ligence	: A Gu	ide for	Thinking	Huma	ns by P	enguin	M	elanie Mi	tchell				
2.	Books, Cyber I		Moralit	y and I	_aw in (Cyberspa	ace, 7th	Edition	1 (2023)	R	ichard Spi	nello. Jone	es & Bar	tlett I	earni	ng
Reference	•			· · · · · ·		, r	, ,		\/	1	~ r	- ,				ی
S.No		Boo	ok Title	e with 1	publica	tion age	ncy &	year		A	uthor					
1.	Artifici	al Intel	ligence	and Et	hics by	, BPB Pu	ıblicatio	ons, 202	23.	S.	B. Kishor	, Debajit 1	Biswas			
2.	Cyber S	Security	and C	yber La	aws by,	Cengage	e India,	2022.		A	lfred Basta	a, Nadine	Basta, S	attwik	Pand	la
	1									I						

NPTEL/ Y	ouTube/ Faculty Video Link:
1.	https://www.youtube.com/watch?v=VqFqWIqOB1g
2.	https://www.youtube.com/watch?v=hVJqHgqF59A
3.	https://www.youtube.com/watch?v=O5RX_T4Tg24
4.	https://www.youtube.com/watch?v=RJZ0pxcZsSQ

Course Cod	e: BASC	C0401		C	ourse l	Name:	Emplo	yabilit <u>y</u>	y <mark>Skill</mark> l	Develo	pment -	II	L	T	P	С	
Course Offe	red in: B	.Tech		•									2	0	0	2	
Pre-requisit	e: Basic ı	ındersta	anding o	of elem	entary 1	mathem	atics						'	•			
Course Obj	ectives:																
The objective	e of this c	ourse is	s to dev	elop stu	idents' d	quantita	ative ap	titude a	nd logi	cal reas	oning sk	ills throug	gh numbe	er theory	, anal	ytica	
puzzles, and	business	mathem	atics, e	nabling	them to	solve i	real-wo	rld and	compet	titive ex	am prob	lems with	speed, a	ccuracy,	and lo	gica	
thinking.																	
Course Out	come: Af	ter com	pletion	of the o	course,	the stud	dent wil	l be ab	le to					n's Knov	vledge	3	
	Apply fundamental number theory concepts such as divisibility. HCE & LCM												Level	(KL)			
CO1	Apply fundamental number theory concepts such as divisibility, HCF & LCM, remain theorem, and cyclicity to solve quantitative problems efficiently.											emainder		K2, K	(3		
											cluding	direction					
CO2											s and cal			K3			
CO3												liscounts,		K2, K	7.2		
		t averaș												K2, N			
CO4	l l					lems in	volving	g aver	ages, m	ixtures	, and rat	ios using		K2, K	[3		
CO-PO Maj		oriate m				Tigh)											
CO-1 O Maj	pping (Sc	ale 1. I	LUW, 2.	Mediu	un, 3. 1	ligii)											
со-ро м	apping	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PS	O2	
CO1		1	1	1	1	-	-	-	-	-	-	-	-	-		-	
CO2	1 1 1 1							-	-	-		-					
CO3		1	1	1	1	-	-	-	-	-	-	-	-	-			
CO4		1	1	1	1	-	-	-	-	-	-	-	-	-		_	
Course Con	tents / Sy	llabus	<u> </u>	1		<u> </u>	<u> </u>	<u>I</u>	<u> </u>	<u> </u>	l	1		1			
Module 1				Spee	d Matl	and N	lumber	Syster	n						8 hou	ırs	
Classification	n of num	ber, Di	visibilit	y Rule,	, Factor	rization	, HCF	& LCN	I, It's	Applica	tion, Mo	dule digi	it(Cyclici	ty), Last	two	digi	
Remainder tl	neorem, F	actoria	l and N	umber (of zeroe	es, High	nest pov	ver									
Module 2				A a 1	41		ai aal D								8 hou		
				1			gical R								8 nou	irs	
Direction and	d Sense, I	3lood R	elation	, Numb	er Serie	es and I	Letter S	eries, C	oding I	Decodir	ıg,						
Module 3				Busin	ness M	ath I									8 hou	ırs	
Percentage, l	Profit and	Loss. I	Discour				Compo	ound In	terest. A	Average	3						
Module 4	10110 0110	2000, 1	2100041		ness M		Comp	7 (411 (4 111	101000, 1	1,0108					8 hou	ırs	
Ratio & Prop	ortion, P	artnersh	nip, Mix	kture &	Allega	tion, Cl	ock, C	alendar						•			
												Total l	Lecture 1	Hours 3	32 hou	urs	
Ref	erence B	ooks:															
S.No	Boo	k Title									Aut	hor					
													C publica	tion co	Pvt I	td)	
ı	Quicker math M. Tyra (BS											<u> </u>			- · • · L		
1 2	2 Quantitative Aptitude RS Aggarwa																
		ntitativ bal & N			asoning	<u> </u>						Aggarwal Aggarwal					

Course Co	de: BEC04	1 01		C	ourse l	Name:	Analog	and D	<mark>igital (</mark>	Commu	nication		L	T	P	С
Pre-requisite: Basic understanding of signal and systems & mathematics.													3			
Pre-requis	site: Basic ı	ındersta	anding (of signa	l and sy	stems	& math	ematics	S.							
Course Ol	ojectives:															
The object	ive of this c	ourse is	the fur	ıdamen	tal of d	ifferent	analog	and dig	gital mo	dulatio	n and der	nodulati	on techni	ques (AN	1, FM	, PM
	, PSK, DPS			_			_			-				_	d spec	trun
	. Also, the									technic	ques and	error co				
Course O	itcome: Af	ter com	pletion	of the	course,	the stud	lent wil	l be abl	e to				Bloor Level	n's Know (KL)	ledge	;
CO 1	Explain various modulation and demodulation methods of Amplitude Modulation and Angle Modulation.															
CO 2		nent va												K3		
CO 3	Analyz system		effect of	f noise	and ex	plain th	e conce	ept of s	pread s	spectrur	n commi	unication	1	K4		
CO 4		the fun evaluat						eory to	design	various	source	encoding	5	K5		
CO 5	Charac	eterize e	error-co	ntrol co	odes and	d apply	the enc	oding a	nd dec	oding p	rocesses.			K5		
CO-PO M	apping (Sc	ale 1: I	Low, 2:	Mediu	m, 3: I	High)										
со-ро	Mapping	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PS	03
CO1		3	2	-	-	-	-	ı	-	-	-	-	3	-	3	3
CO2		3	3	2	-	-	-	-	-	-	-	-	2	-	3	3
CO3		2	3	2	2	-	-	ı	-	-	-	-	2	-	3	3
CO4		3	3	3	2	-	-	-	-	-	-	-	2	-	3	3
CO5		3	2	1	-	-	-	-	-	-	-	-	2	-	3	3
Course Co	ontents / Sy	llabus		I					I		1	1	I.		1	
Module 1				Anal	og Mo	dulatio	n							:	8 hou	rs
	on to Comi											Demodu	lation, A	angle Mo	dulati	ion:
Module 2				Digit	al Mod	lulation	n							1 :	8 hou	rs
Sampling '	Theorem, P	ulse Co	de Mod					n Multi	iplexing	g (TDM	()					
Digital Co	mmunicat	ion Sys	tem: L	ine cod	ling, Bi	nary A				- `	*	modulati	on, Diffe	erential pl	nase si	hift
keying (DI Module 3	PSK), Quad	rature p	hase sh	_	ng (QP t al Rec e										8 hou	
	nal to Nois	o Dotio	(CNID)				ico Eig	ıra Ca	noont o	f Mata	had Eilta	ra DED	onolysis			
BPSK.									_				-			зк,
Module 4	ectrum Co	111111UIII	icauon		rmatio			specifi	ші (ГП	33), DI	icci seqt	che sp	reau spec		8 hou	rs
	f informati	on: Inf	ormatic					nels, So	ource e	ncoding	g: Shann	on Fano	Coding			
Capacity o	f Additive			Noise	(AWG	N) Cha	nnel: Sl			,	-			·		
Module 5					r corre										hour	
	ecting code															
ietecting a	nd correction	ig capa	omity, L	inear b	TOCK CO	ues: en	couing	anu syr	iurome	uecoan	ig. Conv			Hours 4	_	anre
Fext Book	S:											Total	Lecture	110015 4	05 110	<u> </u>
Text Door	Book Tit	le									Autl	nor				
S.No	Book Title Author												and Dor	ald I Sc	hilling	g
	Principles of Communication Systems", Tata McGraw Hill. Herbert Taub and Donald L. Schilling															
S.No	Principles	Digital a	nd Ana						dition, (Oxford		Lathi	and Doi	iaid L. Sc	11111111	<u> </u>

S.No	Book Title	Author						
1	Communication Systems", 4th Edition, Wiley India.	Simon Haykin						
2	Analog and Digital Communications", 2nd Edition, Tata McGraw-Hill.	H.P.Hsu& D. Mitra						
NPTEL/ Y	outube/ Faculty Video Link:							
1	https://nptel.ac.in/courses/117/101/117101051/							
2	https://www.youtube.com/channel/UCnWGGUyQOZkXylsoI5w-J4Q							
3	https://youtube.com/playlist?list=PLbtX56KUSNwTB 27m6HI52rjk8Mz7v23f&si=0-OZ5ktNwpf0MQ7D							

							-							
CO1	Describe the basics of MOS device and CMOS fabrication steps. K1													
CO2	Explain C	MOS inv	erter and	l its swite	ching cha	aracterist	tics.						K.	3
CO3	Design of	Combina	tional ar	d Seque	ntial MC	S logic o	circuits.						K	4
CO4	Explain ar	d design	dynamic	c logic ci	rcuits.								K	4
CO5	Describe t	ne conce	ot of sem	niconduc	tor mem	ories and	ASIC.						K4	
CO-PO	Mapping (S	Scale 1: I	Low, 2: I	Medium	, 3: High	1)								
CO-PO Mappin	POI	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	3	2	-	-	-	-	-	-	-	-	3	-	-
CO2	3	2	3	-	-	-	-	-	-	-	-	3	-	-
CO3	3	3	2	-	-	-	-	-	-	-	-	3	2	-
CO4	3	1	2	-	-	-	-	-	-	-	-	3	-	2
CO5	3	3	3	-	-	-	-	-	-	-	-	3	-	2
	Contents / S	yllabus		NED :		1.63.6	00.01	• .•					10	,
Module	sign flow: \	W CI P				and CM			•, •	D 1 3.5	20.5 :			hours
	Γ capacitano on Process l			, The CN	MOS n-V	Vell Proc	cess,SOI	•	tion				Q	hours
Module				OS inve										
CMOS in	nverter: Circ	uit opera	tion, DC	transfe	characte	eristics, l	Noise ma	argin: cal	lculation				n of CMO	S
CMOS ir inverter,	nverter: Circ Supply volt	euit opera	tion, DC	transfer ce sizing	charactes. Switch	eristics, l ing chara	Noise ma	argin: cal	lculation				n of CMO	S
CMOS ir inverter,	verter: Circ Supply volt ith delay co	euit opera	tion, DC ng, Devi Power o	transferce sizing	characte S. Switch on of CM	eristics, I ing chara IOS inve	Noise macteristic	argin: cal	lculation time defi				n of CMO y times, i	S
CMOS ir inverter, design w Module a	nverter: Circ Supply volt ith delay co 3 ttional MOS	euit opera age scali nstraints, Logic C	ng, Devi Power of Cor ircuits: (C transferce sizing dissipation the complex complex	characte s. Switch on of CM onal and Logic ci	eristics, I ing chara IOS inve sequent ircuits de	Noise macteristic exteristic exter. ial MOS	argin: cal :: Delay t S logic ci Realizing	lculation time defi trcuits Boolear	n express	alculatio	n of dela	n of CMO y times, i	oS nverter hours
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Course Name: CMOS Digital Integrated Circuit

Course Objectives: The students will learn about the basics of MOS device, CMOS fabrication steps, CMOS characteristics. They will learn to apply the knowledge of basic CMOS cell to implement and design combinational and sequential circuits and will understand the concepts of dynamic CMOS logics and semiconductor memories. Students will also be introduced with the concept of

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Bloom's Knowledge

Level (KL)

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Course Code: BEC0403

Course Offered in: B.Tech ECE/VLSI

Pre-requisite: Basis knowledge of MOSFET and Digital Electronics

FPGA implementation of all the logics covered during the full course.

Course Outcome: After completion of the course, the student will be able to

3	"Principles of CMOS VLSI Design" Addison Wesley, Latest Edition.	Weste and Eshraghian			
Refer	ence Books:				
G.M.	D. 1 790				
S.No	Book Title	Author			
1	"CMOS VLSI Design".	Weste and Harris			
2	"Essentials of VLSI Testing for digital, memory and mixed-signal VLSI Circuits", Kluwer Academic Publishers.	Bushnell and Agrawal			
NPTEL/	Youtube/ Faculty Video Link:				
Module 1	https://onlinecourses.nptel.ac.in/noc20_ee29/preview				
Module 2	https://www.youtube.com/watch?v=MuBiC9yz2fc				
Module 3	https://nptel.ac.in/courses/108/106/108106158				
Module 4	https://www.youtube.com/watch?v=UuafwIJAKhY				

Course Offered in: B.Tech ECE/VLSI 3 0 0 3 **Pre-requisite:** Basics of digital electronics Course Objectives: Students will learn about The fundamentals of general microprocessor & microcontroller, The fundamentals of 8086 microprocessor, The architecture of 8051 microcontroller with real time application, The fundamentals of ARM Processor and embedded systems, The knowledge of ARM Instruction Set for programming. **Course Outcome:** After completion of the course, the student will be able to Bloom's Knowledge Level (KL) CO₁ Explain the fundamentals of general microprocessor & microcontroller. K2 CO₂ Explain the fundamentals of 8086 microprocessor. K5 CO₃ Implement 8051 microcontroller for designing various applications. K3 Illustrate the fundamentals of ARM Cortex M0 Processor. **CO4** K4 **CO5** Apply the knowledge of ARM Instruction Set for programming. K4 CO-PO Mapping (Scale 1: Low, 2: Medium, 3: High) PO1 PO2 PO3 COs PO4 | PO5 | PO6 **PO7** PO8 **PO9 PO10** PO11 PSO₁ PSO₂ PSO₃ 3 2 3 2 BEC0402.1 3 1 3 2 3 BEC0402.2 3 1 3 2 3 3 BEC0402.3 3 3 2 2 -_ 3 3 3 3 BEC0402.4 1 2 2 BEC0402.5 3 3 3 2 2 2 Course Contents / Syllabus Module 1 **Basics of Microprocessor and microcontrollers** 8 hours History and Evolution of Microprocessor and microcontrollers, Computer architecture: Harvard & Von Neumann architecture, RISC & CISC architecture, Different Layers of computer architecture, Buses, types of buses, bus architecture, Microprocessor architecture and its operations, address and data bus Multiplexing and Demultiplexing, Instruction format and size. Module 2 **Introduction to 8086** 8hours Introduction to 8086 - Microprocessor architecture, Pipelining Concept, Memory Segmentation, General Purpose Registers, Pointer and Index Registers, Flag Register, Bus Interface Module, 8086 Pin Description, addressing modes, Instruction set and assembler directives, 8086 Interrupt -Software and Hardware Interrupts. **Introduction to 8051** Module 3 8 hours Overview of the 8051, Inside the 8051, Addressing modes, 8051 data types and directives, Instruction set and assembly language programming of 8051 microcontrollers, Programming the 8051 timers, Interfacing of I/O devices (keypad & display) with 8051. Application of 8051 microcontroller. Module 4 **ARM Processor1** 8 hours Arm Processor Families, Arm Cortex-M Series Family, Cortex-M0 Processor: Cortex-M0 Overview, Cortex-M0 Block Diagram, Cortex-M0 Three-stage Pipeline, Cortex-M0 Registers, Cortex-M0 LR, Cortex-M0 PSRs, Cortex-M0 Memory Map, Cortex-M0 Executable Memory Space, Cortex-M0 Device Memory Space, Cortex-M0 Private Peripheral Bus, Cortex-M0 Reserved Memory Space, Cortex-M0 Memory Map Example, Cortex-M0 Endianness. **ARM Processor2** Thumb Instruction Set, Thumb-2 Instruction Set, Cortex-M0 Instruction Set, Register Access: The Move Instruction, Memory Access: The LOAD Instruction, The STORE Instruction, Stack Access: PUSH and POP, Arithmetic instructions (ADD, SUB, MUL, CMP), Logic Operation, Arithmetic Shift Operation, Logical Shift Operation, Rotate Operation, Reverse Ordering Operation, Sleep Mode Related Instructions, CortexM0 Low Power Features: Sleep Mode, Sleep-on-Exit Feature, How to Enable Sleep Features, Processor Wakeup Conditions, Wakeup Interrupt Controller, Enter and Exit Deep Sleep Mode.

"Microprocessor Architecture, Programming, and Applications with the

8085", 5th Edition, Penram International Publication (India) Pvt. Ltd.

Course Name: Microprocessor & Microcontroller

 \mathbf{C}

Total Lecture Hours

Author

Ramesh Gaonkar

40 hours

Course Code: BEC0402N

Textbook:

S.No

2	"Microprocessors and Interfacing", Tata McGraw Hill	Douglas V. Hall		
3	"The 8051".	Mazidi Ali Muhammad, Mazidi Gillispie		
		Janice, and McKinlay Rolin D		
Refe	rence Books:			
S.No	Book Title	Author		
1	Microcontroller and Embedded Systems using Assembly and C", Pearson Publication.	Mazidi Ali Muhammad, Mazidi Gillispie Janice, and McKinlay Rolin D		
2	ARM system developers guide, Elsevier, Morgan Kaufman publishers, 2008.	Andrew N Sloss, Dominic Symes and Chris Wright		
NPTEL/	Youtube/ Faculty Video Link:	-		
Module	1 https://www.youtube.com/watch?v=xBYhHC8_A6o			
Module	2 https://www.youtube.com/watch?v=cNN_tTXABUA			
Module	3 https://www.youtube.com/watch?v=sLW1TptEJBQ			
Module 4	4 https://www.youtube.com/watch?v=9zOo4JkZgSI			
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2	Robotics, Addison-Wesley, 1986.	J.J. Craig
3	Robotics, McGraw Hill, 1987.	K.S Fu, R.C. Gonzalez, C.S.G. Lee
NPTEL/ Y	outube/ Faculty Video Link:	
Module 1	https://www.youtube.com/watch?v=P_PP76flZfw	
Module 2	https://www.youtube.com/watch?v=XOg1KT6xD04&list=PLyqSpQzTF	E6M_XM9cvjLLO_Azt1FkgPhpH&index=5
Module 3	https://www.youtube.com/watch?v=ksOgvhYdqX8	
Module 4	https://www.youtube.com/watch?v=Gc4BiUGiV-Q	
Module 5	https://www.youtube.com/watch?v=pSEjWxqE3R0	

	e: BEC			Cou	irse Nar	<mark>ne: Arti</mark>	ficial In	telligen	ce			L		P	C	
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Course Obj						-			_	•			-			
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assembling			ncrete co	omputati	onal pro	oblems.	They	will acq	uire the	knowled	ge of var	rious forr	ns of lea	arning	an	
computation																
Course Out	come: A	fter con	npletion	of the co	ourse, the	e student	t will be	able to				Bloom's Knowledge Level (KL)				
CO1	Elabora	ate histo	rical per	spective	of AI ar	nd its fou	ındation	s.				K1				
CO2	Apply principles of AI toward problem solving and drawing inference thereof. Describe perception, knowledge representation, and different learning techniques.												K4			
CO3													K3			
C O4	system	s.									her expert		K5			
CO5			nary con				nd differ	ent searc	ch algori	thms.			K5			
CO-PO Ma	pping (S	cale 1:	Low, 2:	Mediun	n, 3: Hig	gh)										
CO-PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PS	03	
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CO3	3	3	3	-	-	-	-	-	-	-	-	2	3			
CO4	3	2	2	-	-	-	-	-	-	-	-	3	3			
CO5	3	3	3	3	ı	-	-	-	-	1	-	3	3		1	
Course Con	tents / S	yllabus	l													
Module 1			Intro	duction	to Arti	ficial In	telligen	ce					8 h	ours		
Historical de																
Intelligent A	gents: C	haracter					al Intell	igent Ag	ents, Pro	blem Sol	ving Appr	oach to T			em	
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problems, ad			Jeuristic													
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Referen	ce Books:	
S.No	Book Title	Author
1	"Artificial Intelligence", Pearson Education Inc., Third edition.	Patrick Henry Winston
2	Python Machine Learning: Learn Python in a Week and Master It. A Hands-On Introduction to Artificial Intelligence Coding, a Project Based Guide with Practical Exercises (7 Days Crash Course, Book2) 2020.	Computer programming Academy
NPTEL/ Yo	utube/ Faculty Video Link:	
Module 1	https://nptel.ac.in/courses/106102220	
Module 2	https://nptel.ac.in/courses/106102220	
Module 3	https://nptel.ac.in/courses/106102220	
Module 4	https://nptel.ac.in/courses/106102220	
Module 5	https://nptel.ac.in/courses/106102220	

Course Code: BEC0	413				Cour	se Nam	e: VLS	I Techn	ology		I	. T	P	C			
Course Offered in: B	.Tech										3	3 0	0	3			
Pre-requisite: Basic l	knowled	lge of S	emicond	luctor d	levices						•	•	•	•			
Course Objectives:	This co	ourse p	rovides	an inti	oductio	n to the	e princ	iples an	d proce	esses of	microfab	rication,	with a f	ocus on			
semiconductor materi	als and	devices	. Studei	nts will	learn a	bout the	e key st	eps in 1	microfat	rication,	such as	photolith	ography,	etching			
deposition, and diffusi	on. The	y will al	so learn	about t	he prope	erties of	semico	ductor	material	s and hov	v they are	used to f	abricate e	lectronic			
devices.																	
Course Outcome: Af	ter com	pletion	of the co	ourse, tl	ne stude	nt will b	e able t	0			Bloom's Knowledge Level (K						
CO1			Inderstand the basic principles of microfabrication.									K4					
CO2					ment mi				K3								
CO3					conduct]	K4				
CO4		_	pply m vices.	icrofab	rication	techni	ques t	o fabri	cate el	ectronic]	K3				
CO5	Know O-PO Mapping (Scale 1: Low, 2: Med						n the fa	bricatio	n proces	SS.]	K4				
CO-PO Mapping (So	ale 1: I	Low, 2:	Mediun	n, 3: H	igh)												
CO-PO Mapping	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3			
BEC0413.1	3	2	1	2	2	1	2	1	-	2	1	2	3	2			
BEC0413.2	3	2	3	2	3	2	2	2	1	2	2	3	3	2			
BEC0413.3	3	2	2	3	3	2	1	1	-	1	1	2	3	2			
BEC0413.4	3	2	3	3	3	2	2	2	1	2	2	2	3	2			
BEC0413.5	2	1	1	1	2	3	3	2	1	1	1	2	2	2			
Course Contents / Sy	llabus								•		•			•			
Environment for VLS Impurity incorporation	I Techno	State di		om and	safety re	equirem	ents. W	afer clea	aning pr	ocesses a		nemical e		hniques			
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2	Fundamentals of microfabrication (2nd ed.). Boca Raton,FL: CRC Press. (2002).	Madou, M. J.
3	Introduction to microelectronic fabrication (2nd ed.). Upper Saddle River, NJ: Prentice Hall. (2002).	Jaeger, R. C.
4	Physics of semiconductor devices (3rd ed.). Hoboken, NJ: Wiley. (2006).	Sze, S. M., & Kwok, K. N.
NPTEL/ Youtube/ Faculty V	Video Link:	
Module 1	https://archive.nptel.ac.in/noc/courses/noc15/SI	EM1/noc15-ec02/
Module 2	wNncTEEcG9zAzEEdnRpZAMEc2VjA3Bpdn	lt=AwrjbCfLAhtoPicCgpRXNyoA;_ylu=Y29sb M-?p=VLSI+Technology&fr2=piv- vid=5e694387d34857a70efe44d25f2595c7&actio
Module 3	wNncTEEcG9zAzEEdnRpZAMEc2VjA3Bpdn	rlt=AwrjbCfLAhtoPicCgpRXNyoA;_ylu=Y29sb M-?p=VLSI+Technology&fr2=piv- &vid=5fa3bdf0373ac3724665542bdfb6fb3d&acti
Module 4	https://nptel.ac.in/courses/117101106	
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Course Co	ode: BAS	0403			Course	Name: A	Advance	ed Engin	eering N	Tathema	tics		L	Т	P	С
Course O	ffered in:	B.Tech.		<u> </u>									3	1	0	4
Pre-requi	site: B.Te	ch 1st ve	ear									<u>l</u>				
Course O				this cours	se is to fa	amiliariz	e the stud	dents wit	h concer	ts of stat	istical te	chnique	es, co	mple	x vari	ables
and Fourie	er Transfo	rm. It ain	ns to sho	w case t	he stude	nts with	standard	concept	s and to	ols from	B. Tech	to deal	with	adva	nced	level
of mathem	atics and	application	ons that v	would be	essentia	al for the	ir discipl	lines.								
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CO3	3	2	1	2	-	-	-	-	1	1	1	2		1		-
CO4	3	2	2	3	-	-	-	-	2	1	1	2		1		-
CO5	3	2	2	3	1	-	-	-	2	1	1	2		1		-
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Module 1			Sta	tistical T	echniqu	ıes-I									3 hou	rs
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1	Introduction to Probability Models	Ross, Sheldon M
2	Probability, Random Variables and Stochastic Processes	Papoulis, Athanasios
3	Advanced engineering mathematics	Kreyszig, E.
NPTEL/	Youtube/ Faculty Video Link:	
Module 1	https://youtu.be/1MiT06JFNo4?si=zVH-5AdAeu7Qcs9x https://youtu.be/6lQn1hdG43o?si=2WJXQHXJE-ByAghk https://archive.nptel.ac.in/courses/110/107/110107114/	
Module 2	https://archive.nptel.ac.in/courses/111/104/111104032/	
Module 3	https://archive.nptel.ac.in/courses/111/107/111107056/	
Module 4	https://archive.nptel.ac.in/courses/111/103/111103070/	
Module 5	NPTEL :: Mathematics - NOC:Integral Transforms And Their Ap	pplications

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CO2	Analyze													K	[4	
CO3	Impleme														6	
CO4							rite the p	rogram f	for given	applicati	ion.			K	[3	
CO-PO M	lapping (S	Scale 1:	Low, 2:	Medium	, 3: Hig l	<u>h)</u>				_						
CO-PO Mapping	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO	1 I	SO2	PS	SO3
CO1	3	3	3	-	3	-	-	-	-	-	-	3		3		2
CO2	3	3	3	-	3	-	-	-	-	-	-	3		3		2
CO3	3	3	3	-	3	-	-	-	-	-	-	3		3		2
CO4	3	3	3	-	3	-	-	-	-	-	-	3		3		2
List of Pr	actical's (Indicati	ve & No	t Limite	d To)											
Module 2	To study	8086 m	icroproce	essor sys	tem.										C	O2
Module 2	Write a p	orogram	using 80	86 Micro	processo	or for He	exadecim	al additi	on of tw	o 8-bit N	umbers.				C	O2
Module 2	Write a p	orogram	using 80	86 Micro	processo	or for He	exadecim	al subtra	ection of	two 8-bi	t Numbe	rs.			C	O2
Module 2	Write a p	orogram	using 80	86 Micro	processo	or for He	exadecim	al additi	on of tw	o 16-bit 1	Numbers				C	O2
Module 2	Write a p	orogram	using 80	86 Micro	processo	or for He	exadecim	al subtra	action of	two 16-b	oit Numb	ers.			C	O2
Module 2	Write a p	orogram	using 80	86 Micro	processo	or for ad	dition of	two BC	D numbe	ers.		_			C	O2

CO2

CO2

CO2

CO2

CO2

CO2

CO₂

CO2

CO₂

CO3

Write a program using 8086 Microprocessor for subtraction of two BCD numbers.

To find the smallest number in an array of data using 8086 instructions set.

To find the largest number in an array of data using 8086 instructions set.

To write a program to arrange an array of data in ascending order using 8086.

To write a program to arrange an array of data in descending order using 8086.

To convert given ASCII number in to its equivalent Hexadecimal number using 8086 instructions set.

To convert given Hexadecimal number in to its equivalent ASCII number using 8086 instructions set.

Write a program to find smallest and largest number in the array using 8051 microcontroller.

To perform multiplication of two 8-bit numbers using 8086.

To perform division of two 8-bit numbers using 8086.

Module

2 Module

2 Module

Module

2 Module

2 Module

2 Module

2 Module

2 Module

Module

3

Module 3 Write a program to arrange numbers in ascending and descending order using 8051 microcontrolle	er. CO3
Module 3 Write a program to find addition and subtraction of two 8 bit numbers using 8051 microcontroller.	: СОЗ
Module 3 Write a program to find multiplication and division of two 8 bit numbers using 8051 microcontrol	ller. CO3
Module 3 Write a program to square of a 8 bit numbers using 8051 microcontroller.	CO3
Module 3 Write a program to cube of a 8 bit numbers using 8051 microcontroller.	CO3
Module 3 Write a program of flashing LED connected to port of the 8051 microcontroller.	CO3
Module 3 Write a program to generate 10 kHz square wave using 8051 microcontroller.	CO3
Module 3 Write a program to generate a Ramp waveform of 1 KHz using DAC with 8051 micro controller.	CO3
Module 3 Write a program to show the use of INT0 and INT1 of 8051 microcontrollers.	CO3
Module Interfacing of sensors and display devices like Serial Communication Code, Bluetooth, seven seg with 8051 microcontrollers.	gments CO3
Module 3 Interfacing of Relay & Stepper Motor with 8051 microcontrollers.	CO3
Module 4 Write and simulate a program for data transfer using ARM freedom board.	CO4
Module 4 Write and simulate a program for arithmetic operations using ARM freedom board.	CO4
Module 4 Write and simulate a program for logical operations using ARM freedom board.	CO4
Module Write a program for Interfacing of temperature sensor with ARM freedom board (or any other AR microprocessor board) and display object temperature on LCD.	CO4
Module 4 Write an embedded C program to blink the LED with time delay intervals using LPC2148 ARM microcontroller.	CO4
Module Write an embedded C program to read switch status and display in LED using LPC2148 ARM microcontroller.	CO4
Module Write an embedded C program to ON/OFF buzzer with time delay intervals using LPC2148 ARM microcontroller.	1 CO5
Module 5 Write an embedded C program generate a square wave using internal 10 bit DAC using LPC2148 microcontroller.	ARM CO5
Module Write an embedded C program generate a triangular wave using internal 10 bit DAC using LPC21 microcontroller.	148 ARM CO5
Module 5 Write an embedded C program generate a PWM waveform using LPC2148 ARM microcontroller.	CO5
Module 5 Write an embedded C program to transmit and receive data from PC using UART serial port using ARM microcontroller.	g LPC2148 CO5
Module 5 Write an embedded C program to read on-chip ADC value of temperature sensor LM35 and displaterminal using UART1 using LPC2148 ARM microcontroller.	ay in hyper CO5
Module Write an embedded C program to read the external interrupts INT1 and INT2 and display in hyper using UART1 using LPC2148 ARM microcontroller.	r-terminal CO5
Module 5 Write an embedded C program to toggle relays with delay intervals using LPC2148 ARM microcol The string CART I using LI C2148 ARM microcol The string CART	ontroller. CO5
Module 5 Write an embedded C program to control the stepper motor using LPC2148 ARM microcontroller	r. CO5
	Total Hours: 40 hrs.

LAB Course C	Code: B	EC045	51N		LAB (Lab	Course	Name:	Analo	g and l	Digital (Commun	ication	L	T	P	C
Course Offere	d in: B	.Tech		<u> </u>									0	0	2	1
Pre-requisite:	Basic k	nowled	dge of a	nalog a	nd digit	tal com	munica	tion co	ncepts					•		
Course Object																
Amplitude mod																
converters like																
communication software.	systen	n and v	arious b	and-pa	ss digit	al modi	ilation	technic	ues, Ir	ne simula	ation of c	convoluti	onal codi	ing using	MAI	.LAI
Course Outco	me: Af	ter com	pletion	of the c	ourse,	the stud	ent wil	l be ab	e to				Bloom	's Know	ledge	
CO1		onstrate modula	-	rform a	mplitu	de mod	ulation	(AM),	frequer	ncy mod	ulation (FM) and		K3		
CO2	Demo	onstrate	and per	rform P	ulse Co	ode Mo	dulation	ı (PCM	[).					K4		
CO3			decode (ent data	ı forma	ts.					K3		
CO4			ital mod											K4		
CO5			volution				AB.							K4		
CO-PO Mapp	ing (Sc	ale 1: l	Low, 2:	Mediu	m, 3: F	Iigh)	ı		1	1	1	ı	Ι	T		
CO-PO Mapping			PO3		PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO 1	PSO 2	P	SO 3
AEC 0451.1	3	2	1	2	-	-	-	-	-	-	-	3	2	2	-	1
AEC 0451.2	3	2	1	2	-	-	-	-	-	-	-	3	2	2		1
AEC 0451.3 AEC 0451.4	3	2 2	1	2	-	-	-	-	-	-	-	3	2	2		1
AEC 0451.4 AEC 0451.5	3	2	1	2	-	-	-	-	-	-	-	3	2 2	2 2	-	1
List of Practic Module 1	Demo	onstrate diode	e amplitu detector	ide mo	dulation nodulat	n by usi ing freq	uency	$f_{\mathbf{m}} = 1$	KHz - 3	3 KHz aı	nd carrie	r frequen	tion by us	0	CC	 D1
	and T Demo	ransmi onstrate	tted Pover	ver (Pt)	dulatio	n and de	emodul	ation (ı	sing PI	LL 565)	with mod	dulating t	Power (F	fm		
Module 1 Module 2	frequ	ency de	eviation	(iii)Mo	dulatio	n index	(β).						Determine ulation wi		CC)1 ——
Module 2	modu	lating t	frequenc	y fm=	80 KH	z.							ZZ & NRZ		CC	
Module 2	Line	Coding	<u>.</u>		-			•				-	& NRZ Li		CC	
Module 2	Codin	ıg.			•			•					r line cod		CC	
	techn				1			1						8	CC	12
Module 2	1010 Deter	1010 w mine E	ith carri Energy p	er frequ er bit (I	iency fo Eb) (iii)	c = 20 k Bandw	:Hz – 1 vidth (B	MHz. (W)	i) Draw	v and obs	serve its		aveform (CC)2
Module 2	with o	carrier (iii) Ba	frequence ndwidth	ey fc = (BW)	940Hz. for FSI	(i) Dra	w its ou	ıtput w	aveforn	n (ii) De	termine l	Energy p	nal 10101 er bit (Eb) for	CC)2
Module 2	carrie	r frequ		= 1.44N	ИНz. (i) Draw							0101010 bit (Eb) f		CC)2

Demonstrate Quadrature Phase Shift Keying (QPSK) modulator and demodulator for message signal

10101010 with carrier frequency fc = 960kHz. (i) Draw its output waveform (ii) Determine Energy per bit (Eb) for QPSK (iii) Bandwidth (BW) for QPSK

Calculation of BER of BASK using MATLAB.

CO2

CO3

Module 2

Module 3

Module 3	Calculation of BER of BFSK using MATLAB.	CO3
Module 3	Calculation of BER of BPSK using MATLAB.	CO3
Module 4	Perform Huffman Coding for given symbols using MATLAB and calculate efficiency.	CO4
Module 4	Perform encoder of (7, 4) Hamming code using MATLAB	CO4
Module 5	Analysis and performance evaluation of convolutional codes using MATLAB for message code = [1 0 1 1]	CO5
	Total H	lours: 40 hrs.

LAB C	B Course : Code BEC0455 LAB Course Name: Verilog-HDL (Departmental Workshop I						T	P	C			
Course	Course Offered in: VLSI											
Pre-rec	quisite: Hardware coding language)										
Course	Objectives: The course will intro	duce the participa	nts to the ver	ilog hardwar	e description language.	It will h	elp th	em to	1			
learn va	arious digital circuit modeling issu	es using verilog, w	riting test be	nches, and so	ome case studies.		_					
Course Outcome: After completion of the course, the student will be able to								Bloom's Knowledge				
						Leve	el (KL	ر)				
CO1	Develop and identify the suitab	le abstraction level	for a particu	lar digital de	sign		K3					
CO2	Develop verilog codes in gate,	dataflow (RTL) mo	deling level	of abstraction	on.		K3					
CO3	Develop verilog codes in behav	ioral (RTL) model	ing levels of	abstraction			K4					
CO4	Design and verify the functional	lity of digital circu	it/system usi	ng test bench	nes		K	(4				
CO5	Design and simulate basic modules using switch level modeling. K5											
	Mapping (Scale 1: Low, 2: Med		<u> </u>	D								

CO-PO Mapping	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	2	2	-	3	-	-	-	-	2	1	3	-	2
CO2	3	3	2	-	3	-	-	-	-	2	1	3	-	-
CO3	3	2	2	-	3	-	-	-	-	2	1	3	2	-
CO4	3	2	-	-	3	-	-	-	-	2	1	3	-	2
CO5	2	3	2	-	2	-	-	-	-	2	1	3	-	2

Evolution of CAD, emergence of HDLs, typical HDL-flow, trends in HDLs, Verilog vs VHDL, Verilog oding vs Software Programming. Cop-down and bottom-up design methodology, differences between modules and module instances, parts of simulation, design block, stimulus block. Lexical conventions, data types: value set, registers, vectors, arrays, strings, system tasks, compiler lirectives. Module definition, port declaration, connecting ports, hierarchical name referencing Modeling using basic Verilog gate primitives, description of and/or and buf/not type gates, rise, fall and turn-off delays, min, max, and typical delays. Continuous assignments, delay specification, expressions, operators, operands, operator types.	15 Hour
off delays, min, max, and typical delays.	
continuous assignments, detay specification, expressions, operators, operator types.	
Structured procedures, initial and always, blocking and non-blocking statements, delay control, generate statement, event control, conditional statements, Multiway branching, loops, sequential and parallel blocks.	20 11
Timing and Delays, Switch-Level Modeling, Logic Synthesis with Verilog HDL, Specify block and Timing checks, Verification and Writing test benches, Timing Analysis of Logic circuits, Downloading of verilog code in FPGA and CPLD.	
Concept of switch level abstraction, MOS Transistor as Switch, Modeling NMOS and PMOS transistors as switches in Verilog, Switch ON/OFF conditions and control signals, Verilog Switch-Level Primitives, Understanding Verilog switch primitives: nmos, pmos, Syntax and usage of switch primitives in Verilog code.	20 Hour
Fin Co Mo Sw	ming and Delays, Switch-Level Modeling, Logic Synthesis with Verilog HDL, Specify block and Timing ecks, Verification and Writing test benches, Timing Analysis of Logic circuits, Downloading of verilog de in FPGA and CPLD. Incept of switch level abstraction, MOS Transistor as Switch, odeling NMOS and PMOS transistors as switches in Verilog, witch ON/OFF conditions and control signals, Verilog Switch-Level Primitives, Understanding Verilog

Lab No.		Program Logic Building	CO Mapping
1	Simulate and synthesize f a) AND Gate b) OR Gate c) NOT Gate d) EX-OR Gate e) NAND Gate f) NOR Gate	ollowing logic gates using gate level modeling	CO1
2	Simulate and synthesize f a) Half adder b) Full adder c) Half subtractor d) Full subtractor e) 4:1 Multiplexer f) 4:2 Encoder g) 1:4 Demultiplexer h) 2:4 Decoder i) 1 Bit Comparator j) 2*2 Bit Multiplier	ollowing combinational circuits using gate level modeling	CO2
3		size binary to gray code converter using gate level modeling. size gray to binary code converter using gate level modeling.	CO 2
4	a) Half adder b) Full adder c) Half subtractor d) Full subtractor e) 4:1 Multiplexer f) 4:2 Encoder g) 1:4 Demultiplexer h) 2:4 Decoder i) 1 Bit Comparator j) 2*2 Bit Multiplier	ollowing combinational circuits using data flow modeling	CO 2
5		bit parallel adder/subtractor using data flow modeling.	CO 2
6	OPCODE 1. 2. 3. 4.	ALU Operation A+B A-B A Complement A*B	CO 2
7		size binary to gray code converter using data flow modeling. size gray to binary code converter using data flow modeling.	CO 2
8	Simulate and synthesize f a) SR Flip Flop b) JK Flip Flop c) D Flip Flop T Flip Flop	ollowing flip flops using behavioral modeling	СОЗ
9	Simulate and synthesize f a) Using positive edge	lip flops using behavioral modeling and negative edge. nd asynchronous reset	CO3

10	Simulate and synthesize following shift registers using behavioral modeling	
	a) Serial input serial output	
	b) Serial input parallel output	CO3
	c) Parallel input serial output	
11	d) Parallel input parallel output	
11	Simulate and synthesize following universal shift register using behavioral modeling	CO3
12	Simulate and synthesize following counters using behavioral modeling	
	a) 2 Bit Counter	
	b) Mod 5 Counter	CO3
	c) Decade Counter	
	d) Ring Counter	
10	e) Johnson Counter	
13	Simulate and synthesize array multiplier using behavioral modeling	CO3
14	Simulate and synthesize 4:1 MUX by using 2:1 MUX	
	a) Using a wire	CO3
	b) Using a reg	
15	Simulate and synthesize Moore sequence	COA
	a) 1010 b) 1011	CO3
16	Simulate and synthesize Mealy sequence	
10	a) 1010	CO3
	b) 1011	
17	Implementation of logic gates on an FPGA and verify gates functionality.	CO 4
18	Implementation of 4:1 multiplexer on a FPGA	CO 4
19	Implementation of 2*2 multiplier on a FPGA	CO 4
20	Implementation of D flip flop on a FPGA	
20	Implementation of B mp nop on all Fort	CO 4
21	Design and simulation of CMOS inverter using switch level modeling	CO 5
22	Simulate and synthesize following logic gates using switch level modeling	
	a) AND Gate	
	b) OR Gate	
	c) NOT Gate	GO =
	d) EX-OR Gate	CO 5
	e) NAND Gate	
	f) NOR Gate	
	Required Software and Tools (Any one)	
•	ISE Simulator (Xilinx) / Xilinx Vivado	
•	Verilog-XL (Cadence)	
•	VCS ('big 3') (Synopsys)	
		70 4 1 40

Total: 40 hrs

LAB Course Code: BCSCC0452	LAB Course Name: Problem Solving Approaches	L	T	P	С
Course Offered in: IV SEM		0	0	2	1

Pre-requisite: Programming Language C/C++ or Java or Python

Course Objectives:

Problem-solving in computer programming involves a structured approach to identifying, analyzing, and resolving coding challenges. The process typically includes thoroughly understanding the problem, decomposing it into smaller, manageable parts, designing an appropriate algorithm, implementing the solution through code, and performing testing and debugging to ensure correctness and efficiency

	- J	
Course	Outcome: After completion of the course, the student will be able to	Bloom's Knowledge
		Level (KL)
CO1	Develop logic-based solutions using control statements and recursion to solve basic and intermediate computational problems.	K6
CO2	Apply bit manipulation techniques to find efficient solutions for binary and low-level operations.	K3
CO3	Implement and manipulate arrays and strings using fundamental and advanced searching sorting techniques.	K3
CO4	Utilize algorithmic strategies to optimize solutions for complex problem scenarios.	K3
CO5	Analyze and debug code for logical errors and improve the efficiency of the solution using appropriate data structures and algorithmic patterns.	K4

CO-PO Mapping (Scale 1: Low, 2: Medium, 3: High)

CO-PO Mapping	PO1		PO3	PO4		PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	3	3	3	-	-	-	2	-	-	-	-	-	-
CO2	3	3	2	2	-	-	-	2	-	-	-	-	-	-
CO3	3	3	2	2	-	-	-	2	-	-	-	-	-	-
CO4	3	3	2	2	-	-	-	2	-	-	-	-	-	-
CO5	3	3	2	2	-	-	-	2	-	-	=	-	-	-

List Of Practical's (Indicative & Not Limited To)

Problem Statements need to be discussed in lab session: Control Statements

1. Secure Password Generator

A company wants to create a secure password generator for their employees. The password must be based on specific numeric properties to enhance its complexity and security. Write a program to validate and generate a secure password according to the following rules:

1. Prime Number Validation:

- The user must input a 3-digit number. The program should first check if the number is a prime number.
- If it is not a prime number, the user should be prompted to enter another number until a valid prime number is provided.

2. Sum of Digits Check:

• Once a valid prime number is entered, calculate the sum of its digits. If the sum of the digits is not divisible by 3, ask the user to enter another prime number until a valid one is found.

3. Armstrong Number Check:

• Check entered prime number is Armstrong or not? If Armstrong are found, prompt the user to enter another prime number and repeat the process.

Password Generation:

Concatenate the 1 if entered prime number is Armstrong otherwise 2 with the sum of the digits of the valid prime number to form the secure password.

Example Scenario:

Sample Input

Enter a 3-digit prime number: 153

Sum of digits of 153 = 9The sum is divisible by 3. 153 is Armstrong number

Sample Output

Secure Password: 19

2. Write a function to input electricity unit charges and calculate total electricity bill according to the given condition:

For first 50 units Rs. 0.50/unit For next 100 units Rs. 0.75/unit For next 100 units Rs. 1.20/unit For unit above 250 Rs. 1.50/unit

An additional surcharge of 20% is added to the bill

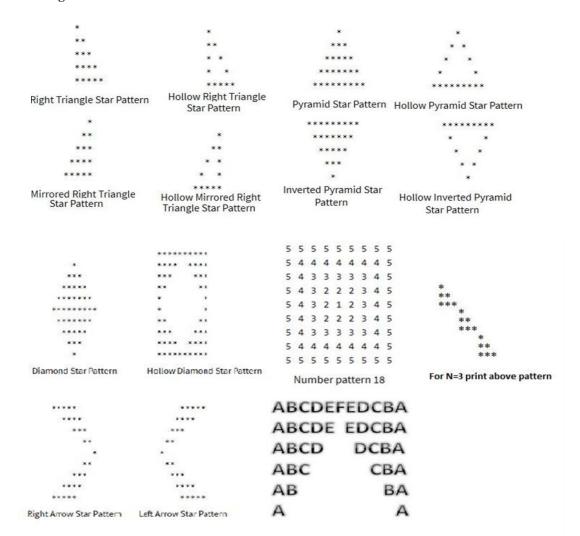
3. Write a method to generate a secure code which the sum of all possible palindrome numbers between given two numbers.

For Example: **Input**: 10, 80 **Output**: 308

Explanation: All palindrome numbers between 10 & 80 are: 11,22,33,44,55,66,77

Password= 11+22+33+44+55+66+77 = 308

4. Draw the following Patterns for N=5



Problem Statements need to be discussed in lab session: Recursive Approach (Basic)

1. Write a program that takes an integer n as input and prints the multiplication table of n from n * 1 to n * 10. The output should clearly show each multiplication step.

2. Write a program to calculate the sum of all integers from 1 to a given number N. The program should take N as input and output the total sum using iteration or recursion.

3. Find the GCD of Two Numbers Using Recursion:

Write a recursive function to calculate the Greatest Common Divisor (GCD) of two numbers using Euclid's algorithm. The function should take two integers as input and return their GCD.

4. Find the LCM of Two Numbers Using Recursion:

Write a program to compute the Least Common Multiple (LCM) of two numbers using recursion. You may use the relationship LCM(a, b) = |a * b| / GCD(a, b) and a recursive function for GCD.

Problem Statements need to be discussed in lab session: Bit Manipulation

- 1. Write a program to count the number of set bits (1s) in the binary representation of a given integer. The program should efficiently use bitwise operations to perform the task without converting the number to a string.
- 2. Write a program that takes a number and a bit position as input and checks whether the bit at that position is set (1) or clear (0). Use bitwise operators to perform the check
- **3.** Given a number and a position, write a program to toggle (invert) the bit at the given position using bitwise operations. The result should reflect the updated value of the number after flipping the bit.
- **4.** Write a program to compute the XOR of all numbers from 1 to n using a mathematical pattern (not a loop). Use bitwise XOR properties to achieve an efficient solution.
- **5.** Given an array of size n-1 containing unique elements from 1 to n, find the missing number using bit manipulation (preferably XOR approach) without sorting or using extra space.
- **6.** Given an array where all elements repeat twice except two elements that appear only once, write a program to find the two non-repeating elements using bitwise operations in linear time and constant space.
- 7. Write a program to check if a given number is a power of two using bit manipulation. A number is a power of two if it has exactly one set bit in its binary representation.
- **8.** Given two integers A and B, write a program to count how many bits need to be flipped to convert A to B. Use XOR to find differing bits and count the number of set bits.
- **9.** Write an efficient program to count the total number of set bits in binary representations of all numbers from 1 to n. Optimize the approach using bitwise logic and recursion.
- **10.** Write a program to calculate the square of a number using only bitwise operations and addition. Do not use multiplication, division, or any power functions.
- 11. Write a function to add two integers using bitwise operations only. Avoid using the + or operators. Implement logic using XOR and AND operations for binary addition.
- **12.** Write a program to generate the power set (all subsets) of a given set using bitwise representation. Each subset can be represented by a binary number where each bit indicates inclusion of the corresponding element.

Problem Statements need to be discussed in lab session: Arrays (Try to use sliding window, prefix sum, cadence, recursion, bit manipulation, two pointer approaches)

- 1. Sarah is assisting the "MathMinds Club" in creating passwords for their online platform. They have a list of numbers, some stable and some unstable. Define a function that can help Sarah calculate the password according to the given scenario. Scenario:
 - There are N numbers provided.
 - A number is stable if each digit appears the same number of times.
 - A number is unstable if the frequency of its digits is not the same.
 - The password is computed as the sum of all stable numbers minus the sum of all unstable numbers.
 - Consider only those numbers in the list that have more than equal to three digits.

For example:

Input: N=5 List: 12, 1313, 122, 678, 898

Output: Password: 971

2. Given an array of integers, including possible negative values, you are allowed to modify at most one element by doubling its value. The goal is to find the maximum possible sum of any subarray after making this modification.

Input:

arr = [-2, 1, -3, 4, -1, 2, 1, -5, 4]

Expected Output:

- Original Maximum Subarray Sum: 6 (achieved from [4, -1, 2, 1])
- Maximum Sum After Modification: 10(achieved from [8, -1, 2, 1], where the value 4 is doubled to 8).
- **3.** For a given string, generate a pattern based on the following rules:

Input: A string of characters (e.g., "HAT").

Output: Generate patterns by replacing characters with the numeric value 1 and process the patterns as described below:

- 1. Replace one character at a time with 1:
 - o For each character in the string, replace it with 1, keeping the other characters unchanged.
 - Example for "HAT": 1AT, H1T, HA1
- 2. Replace two characters at a time with 1:
 - o Replace every combination of two characters with 1, keeping the remaining character unchanged.
 - o If 1s are consecutive, replace them with their sum (e.g., 11T becomes 2T).
 - Example for "HAT":

 $11T \rightarrow 2T$, $H11 \rightarrow H2$, 1A1

- 3. Replace all characters with 1:
 - o Replace all characters in the string with 1.
 - o If there are consecutive 1s, sum them up (e.g., 111 becomes 3).
 - o Example for "HAT":

 $111 \rightarrow 3$

Final Output

For the string "HAT", the output should be:

1AT, H1T, HA1, 2T, H2, 1A1, 3.

4. Given a sorted array arr [] and a target value, the task is to count triplets (i, j, k) of valid indices, such that arr[i] + arr[j] + arr[k] = target and i < j < k.

Examples:

Input: arr[] = [-3, -1, -1, 0, 1, 2], target = -2

Output: 4

- 5. You are given an array prices[] where prices[i] represents the price of a given stock on day i. You want to maximize your profit by choosing a single day to buy one stock and choosing a different day in the future to sell that stock. Write a program to return the maximum profit you can achieve from this transaction. If no profit is possible, return 0.
- 6. Find the "Kth" max and min element of an array:

Given k, find the k-th smallest and k-th largest element in the array.

Input: arr = [7, 10, 4, 3, 20, 15], k = 3 Output: Kth Smallest: 7, Kth Largest: 10

7. Sort a binary array with values 0, 1, and 2 using constant space and one pass (Dutch National Flag algorithm).

Input: [0, 2, 1, 2, 0]Output: [0, 0, 1, 2, 2]

8. Find **longest consecutive subsequence:**

Return the length of the longest consecutive elements sequence.

Input: [1, 9, 3, 10, 4, 20, 2] Output: 4 (Sequence: 1, 2, 3, 4)

9. Given a number of bits and a number K. In one flip you can toggle exactly K consecutive bits. With only this flip operation available, convert the string into all 1.

Input String: 0000110000 and K=3

Following are four flip operations by using which all bits converted into 1's.

Flip1-1110110000 Flip2-1110110111 Flip3-1111000111 Flip4-111111111

If it is not possible to convert all bits into one's then print "IMPOSSIBLE".

10. Given a list of non-negative integers, arrange them in such a way that they form the largest possible number. Since the result can be very large, return it as a string in O(N log N) time complexity.

Example-1	Example-2
Input:	Input:
N = 5	N = 4
Arr[] = {3, 30, 34, 5, 9}	Arr[] = {54, 546, 548, 60}
Output: 9534330	Output: 6054854654

11. Given an array arr[] of size n containing distinct integers within the range [1, n+2], find the two missing numbers from the first n+2 natural numbers.

Constraints:

- The solution must run in O(N) time and use O(1) extra space.
- The array does not contain duplicate values.

Examples:

Input: arr[] = [1, 2, 4, 6, 3, 8], n = 6

Output: 5, 7

12. Given a string str of lowercase alphabets and a number k, the task is to print the minimum value of the string after removal of k characters. The value of a string is defined as the sum of squares of the count of each distinct character present in the string. Return the minimum possible required value. **Examples:**

Input: str = "abccc", k = 1

Output: 6

Input: str = "aabcbcbcabcc", k = 3

Output: 27

Expected Time Complexity: O(n+klog(p))

Note: Here n is the length of string and p is number of distinct alphabets and k number of alphabets to be removed.

13. Given a non-negative integer **S** represented as a string, remove **K** digits from the number so that the new number is the smallest possible.

Note: The given *num* does not contain any leading zero.

Expected Time Complexity: O(|S|).

Example 1:	Example 2:	
Input:	Input:	
S = "149811", K = 3	S = "1002991", K = 3	
Output:	Output:	
111	21	

14. You are given a two-dimensional grid board[][] of size n * m consisting of English letters and a string target. Your task is to determine whether the target word can be formed by sequentially connecting letters from the grid. You may move to adjacent cells **horizontally or vertically** (not diagonally), and **a cell may not be reused** once it is part of the current path.

Examples:

Input:

board[][] = [['C', 'A', 'T'], ['R', 'A', 'K'], ['T', 'O', 'N']],

target = "CART"

Output: true

Explanation:

You can trace the word "CART" through the path: $C \to A \to R \to T$ (moving horizontally and vertically, without repeating cells).

- 15. Given an encoded string s, the task is to decode it. The encoding rule is:
 - k[encodedString], where the encodedString inside the square brackets is being repeated exactly k times. Note that k is guaranteed to be a positive integer, and encodedString contains only lowercase english alphabets.

Note: The test cases are generated so that the length of the output string will never exceed 10^5.

Examples:

Input: s = "1[b]" **Output:** "b"

Input: s = "3[b2[ca]]" **Output:** "bcacabcacabcaca"

*Competitive coding list will be shared with the students.

Total Hours: 30 hrs.

Course (Code:	BNC0402	2 Y	Co	urse Namo	e: Environ	mental Sci	ience		L	T	P	C
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						environmen	tal issues,	conserve b	iodiversity	, and		Know	ledge Leve
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CO2		erstand the servation.	e different	types of na	itural recou	ırses like fo	ood, forest,	Minerals a	nd energy	and the	eir	K1,K2	
соз		erstand the	e different	types of po	ollution, po	llutants, the	eir sources,	, effects an	d their con	trol		K1,K2	
CO4			e basic con-	_		evelopmen	t, Environi	mental Imp	act Assess	ment		K1,K2	
CO-I	PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	РО	9	PO10	PO11
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CO1		3	3	2	2		3	3	2	2			2
CO2		3	3	2	2		3	3	2	2			2
СОЗ		3	3	2	2		3	3	2	2			2
CO4		3	3	2	2		3	3	3	2			2
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Module 2	2		Nat	ural Reso	urces and	Ecological	succession	1				5]	hours
Natural r	esour	ces and as				rces: Use ar			deforestat	ion. Tir	nber (extraction	n, mining,
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Module 3	3		Poll	ution and	Waste Ma	anagement						5	hours

Hydrocarbon, control of air pollution. Water pollution: sources and types of water pollution, Effects of water pollution, Eutrophication, Soil pollution: Causes of soil pollution, Effects of soil pollution, Major sources of and effects of noise pollution on health, Radioactive and thermal pollution sources and their effects on surrounding environment. Solid waste disposal and its effects on surrounding environment, Introduction to E- Waste, Types and classification of E- Waste, Impacts of E- Waste on environment and human health, E-Waste management and recycling., Climate change, global warming, acid rain, ozone layer depletion. **Environmental Assessment and Legislation**

Women education, Role of NGOs regarding environmental protection, Bio indicators and their role, Natural disasters and disasters

management, Aims and objectives of Environmental Impact Assessment (EIA). Salient features of following Acts: Environmental Protection Act, 1986, Wildlife (Protection) Act, 1972. Water (Prevention and control of pollution) Act, 1974. Forest (Conserving) Act, 1980.

Definition and concept of sustainability, impacted areas of sustainable development, Global initiative and issues on sustainable development UNSDsGs, System Thinking and Sustainability.

	Total Lecture Hours 20 hour										
Textboo	k:										
S.No	Book Title	Author									
1	Brady, N.C. 1990. The nature and properties of Soils, Tenth Edition. Mac Millan Publishing Co., New York	Brady, N.C									
2	Sodhi G.S. 2005, Fundamentals of Environmental Chemistry: Narosa Publishing House, New Delhi.	Sodhi G.S									
3	Dash, M.C. (1994), Fundamentals of Ecology, Tata Mc Graw Hill, New Delhi.	Dash, M.C									
S.No											
1	Rao M.N. and H.V.N. Rao, 1989 : Air Pollution, Tata McGraw Hill Publishing Co. Ltd., New Delhi	Rao M.N. and H.V.N. Rao									
2	A Text Book of environmental Science By Shashi Chawla	Shashi Chawla									
Unit 1:	https://www.youtube.com/watch?v=T21OO0sBBfc, https://www.youtube.com/watch?v=T21OO0sBfc, https://www.youtube.com/watch?v=T21OO0sfc, https://www.youtube.com/watch?v=T21OO0sfc, https://www.youtube.com/watch?v=T21OO0sfc, https://www.youtube.com/watch?v=T21OO0sfc, https://www.youtube.com/watch?v=T21OO0s	be.com/watch?v=qt8AMjKKPDo									
Unit 2:											
	https://www.youtube.com/watch?v=yqev1G2iy2										
	https://www.youtube.com/watch?v=_74S3z3IO_I,										
	https://www.youtube.com/watch?v=jXVw6M6m2										
Unit 3:	https://www.youtube.com/watch?v=7qkaz8ChelI,										
	https://www.youtube.com/watch?v=NuQE5fKmfME	/									
TT 1. 6	https://www.youtube.com/watch?v=9CpAjOVLHII, ttps://www.youtube.com/watch?v=yEci6iDkXYw										
Unit 4	https://www.youtube.com/watch?v=ad9KhgGw5iA,										
	https://www.youtube.com/watch?v=nW5g83NSH9 M,										
	https://www.youtube.com/watch?v=xqSZL4Ka8xo										